Buck Converters for Low Power Applications

BY

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To my parents

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All praise be to Allah, and peace and blessings be upon his messenger.

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Finally and most importantly I am forever gratefull to my parents and I pray to Allah that *"... Grant me the power and ability that I may be grateful for Your Favour which You have bestowed upon me and upon my parents, and that I may do righteous good deeds, such as please ... " (Surah Ahqaf: 15)*

Mohanad Ahmed

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THESIS ABSTRACT

NAME:	Mohanad Ahmed Mohamed Elhassan
TITLE OF STUDY:	Buck Converters for Low Power Applications
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Consumer electronics has no doubt entered every aspect of modern life. Scaling of CMOS technologies has provided the platform to serve the ever more increasing demands of consumers: more functionality, higher performance, longer battery lifetime all at lower prices and smaller sizes. Many portable devices have Buck converters that adapt the higher battery or supply voltage to the lower voltage levels demanded by digital circuits.

This thesis explores two topics related to Buck converters. First: the design of buck converters requires the sizing of switches and passive components. Selecting a suitbale design point requires the ability to evaluate the performance at the design point. In this thesis we propose an automated algorithm (called MNA-SS-REDOX) for state space generation and performance evaluation of DC-DC converters (in general). The algorithm is applied to several types of buck converters and compared against simulation results from SPICE found to be in good agreement with the simulation results. The algorithm also sets the stage for an automated optimizer to be used for sizing of components.

Second: the output range over which the buck converter exhibits certain efficiency directly affects the battery lifetime. Portable devices spend considerable amount of time in low power modes. We propose a hybrid buck converter power stage that allows serving of a wide range of loads (100μ - 1A) i.e. a range of 10000. The power stage is

formed of a switched capacitor power stage and an inductive power stage. The output voltages provided by this converter are in the range 0.7 – 1.4V with a peak efficiency of 82%.

مستخلص الرسالة

الاسم	مهند أحمد محمد الحسن أحمد
عنوان الرسالة	محولات بك لتطبيقات القدرة المنخفضة
التخصص	الهندسة الكهربائية
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لقد دخلت الإلكترونيات الحديثة في كافة مجالات الحياة. تعتبر تقنيةCMOS هي التقنية الأكثر استخداما في الإلكترونيات، و قد أدى تصغيرها المتواصل إلى جعلها الأداة الأفضل لتحقيق رغبة المستهلك في أجهزة تحتوي على وظائف أكثر، أداء أفضل و استهلاك أقل للبطاريات و تكلفة أقل. تقوم محولات Buck بتحويل جهد البطارية المرتفع إلى جهد أقل موائم للدوائر الرقمية المستخدمة في هذه الأجهزة

نتطرق في هذه الرسالة إلى موضوعين متعلقين بمحولات Buck الأول: تصميم دوائر المحولات يحتاج من المصمم إلى تحديد أبعاد الترانزيستورات و عناصر الدائرة الأخرى. الإختيار الأمثل لهذه القيم يعتمد على مقدرة المصمم على تقييم أداء المحول عند نقطة معينة. في هذه الرسالة نقترح خوارزمية لتقييم هذا الأداء بصورة أوتوماتكية ابتداء من معطيات الدائرةز تم تطبيق هذه الخوارزمية و مقارنة نتائجها مع نتائج برنامج SPICE و تبين النتائج تقاربا جيدا في النتائج و مقدار خطأ لا يزيد عن ١٪ تمهد الخوارزمية المقترحة أيضا الطريق لأتمتة عملية تحديد الأبعاد بشكل أوتوماتيكي من خلال أي من خوارزميات ال Optimization المعروفة.

ثانيا: يؤثر المدى الذي يغطيه محول بك بكفاءة جيدة على مدة استخدام البطارية من غير شحن. لتحسين المدى نقترح في هذم لرسالة محول بك مدمج مكون من محول يك حثي لتغطية التيارات المرتفعة و محول المكثفات متقطعة التوصيل لتغطية المدى التيارات الأقل. يوفر هذا المحول خرجا بين ط٠.٧ و ط١.٤ بكفاءة قصوى تعادل ٨٢٪.

CHAPTER 1

INTRODUCTION

Consumer electronics has no doubt entered every aspect of modern life. Scaling of CMOS technologies has provided the platform to serve the ever more increasing demands of consumers: more functionality, higher performance, longer battery lifetime all at lower prices and smaller sizes. An essential element of every electronic system are the power management circuits (PMC). In many applications the voltage of the source (battery, energy harvester) is not directly usable by the circuitry, requiring voltage level conversion. The need for conversion is common in portable devices, communication devices and biomedical devices. The need for miniaturizations and lower power consumption has pushed research towards more integration of power management and higher efficiencies.

Although the digital circuits scale with every generation of CMOS technology, the power management circuits have not scaled proportionally. Consider a modern

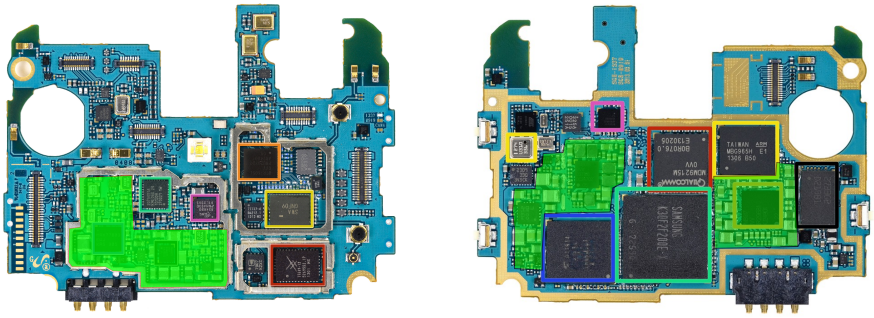


Figure 1.1: Main Electronic Board of Samsung Galaxy S4 from iFxit Teardown. Shaded areas are power management areas (a) Backside (b) Front Side [1]

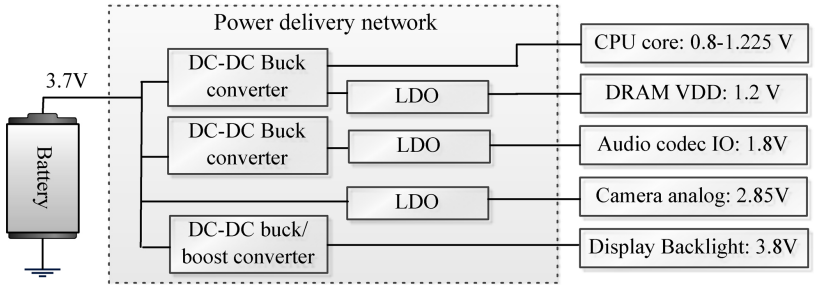


Figure 1.2: Power Delivery Hierarchy in a Battery Power Mobile Device [4]

consumer device like the Samsung Galaxy S4. The front and backsides of the main electronic boards are shown in Figure 1.1. The shaded areas show the power management circuits. They occupy more than 20% of the board area, more than the processor and memory combined. Similar observations apply to other portable devices. [2, 3]

DC-DC Converters perform voltage level conversion in order to "match" the source to the loading circuitry [4]. The conversion can be either step-up or step-down conversion. A typical power management hierarchy is show in Figure 1.2. Buck converters are DC-DC converters that convert from higher DC input voltage to lower output DC voltage. In Figure 1.2 the CPU core and RAM are supplied by buck converters.

Digital circuits (such as CPU and RAM) employ some techniques to reduce power consumption and improve battery lifetime. Examples of such techniques are voltage scaling, power gated domains, Dynamic Voltage Scaling (DVS) and Ultra-Dynamic Voltage Scaling (U-DVS) [5,6]. DVS and U-DVS require a source capable of providing variable voltages. In order not to offset the power savings achieved by DVS a highly efficient and variable converter is required. The efficiency is particularly important in light load for two reasons: first using DVS, the light load period is actually the period of time savings and second in many cases it constitutes a large percentage of the operation time [7]. Figure1.3a shows the residency distribution of a laptop. It is clear that it shows large residence in light load areas. Figure1.3b shows the distribution of current consumption for a processor in a mobile platform. The processor spends more time in light load regions.

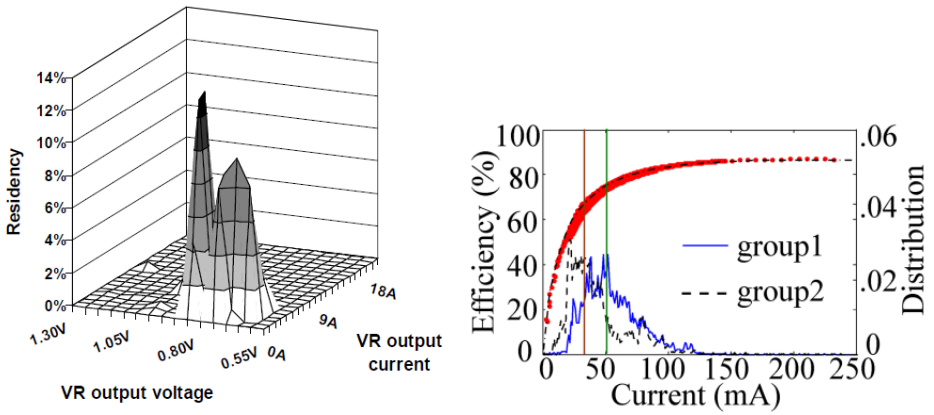


Figure 1.3: (a) Residency percentage of laptop for different voltage and current values [7] (b) Power Consumption distribution and efficiency of processor in a mobile phone [4]

1.1 Performance Metrics of DC-DC Converters

DC-DC Converters are widely used in many applications, each having its own set of different requirements. To evaluate the suitability of a converter for a specific application and compare between DC-DC converters, several parameters are used.

The first parameter is efficiency, defined as the ratio of the average power delivered to the load to the average input power. Efficiency varies with many parameters such as the load on the converter and the output voltage. An often quoted figure to summarize the efficiency information is the peak efficiency. Of course this is not always a true representation of the whole range.

Output range in terms of load current and voltage are another set of parameters. These are usually dictated clearly by the specific application. Transient response is the rate at which the output voltage achieves steady state after a change. This could be a change in: the load (termed a load transient), the reference voltage (known as a reference transient) or a change in the input voltage known as the line transient. Regulation quantifies the ability of the converter to regulate the output voltage to the reference voltage when changes occur in the load current or the input voltage. These are known as load and line regulation respectively.

Noise performance parameters such as output ripple, spectrum distribution of ripple and power supply rejection ratio measure how clean the output voltage is. The

previously mentioned parameters are performance parameters that affect the performance of the system during operation. Converters are also evaluated based on some design parameters. These will affect the incorporation of the converter in a complete system. Examples of such design parameters are: chip area, pin count, possibility of direct battery connection [5], [6].

One of the most important design parameters is the level of integration. Current designs available are classified into either monolithic (everything on one die), fully integrated (everything on chip; may use off die components) and finally requiring of chip components. Full integration of the converter components allows it to be placed on the same ship as the rest of the circuitry or system, as such reducing costs, pin counts and the overall footprint of the system. On the other hand this imposes several challenges on the designer such poor quality and small size of on chip components, analog on-friendly characteristics of the deep submicron technologies, in addition to the challenges faced by IC designers such as limited area.

The above discussion highlights a common issue in many analog and mixed signal design problems: the number of requirements and evaluation parameters is relatively large (compared to purely digital design) and as such is believed to be more challenging.

1.2 Types of DC-DC Converters

There are three main types of DC-DC Converters: Linear Dropout Regulators, Switched Capacitor Converters and Inductive Converters. The first, Linear Dropout (LDO) Regulators, utilize a resistive drop top reduce the voltage to the load expected output voltage. Usually the resistor is implemented as a transistor. A high gain amplifier usually closes the loop between the output and the gate of the drop transistor providing regulation, Figure1.4. This type of converter has many advantages including its fast transient response, stability, very small ripple, small area and till recently has been the dominant regulator. However its main issue is low efficiency for low conversion ratios. The efficiency is inherently limited by the conversion ratio (output voltage /

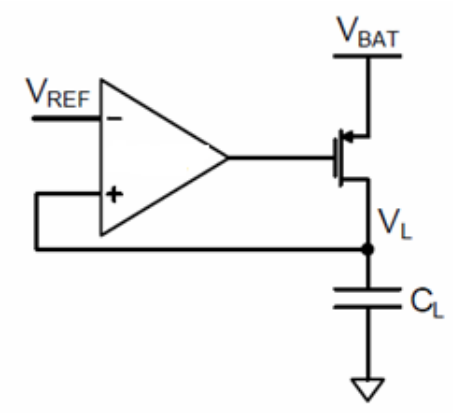


Figure 1.4: LDO Regulator with capacitor at output and amplifier for regulation. [8]

input voltage). Since this converter has been the standard for some time it has been used as a benchmark for other converters. Efficiency Enhancement Factor (EEF) gives the enhancement of another converter relative to an ideal LDO of the same conversion ratio. Of course LDOs are by design only step down converters.

The other two types are switched capacitor (SC) and inductive switching converters. These two types employ switches and passive elements (inductors and capacitors) to achieve conversion. Switched capacitor converter circuit employ only capacitors and switches. One capacitor is connected across the load. Switched capacitor converters in their simplest form operate by dividing the time into periodic intervals. Further each interval is divided into two phases. In phase 1 several capacitors are connected in some combination across the input. Each charges to some specific level. In phase 2, through switches, the circuit is disconnected from the source and rearranged across the load capacitor with a predetermined ratio. Charge is transferred to the load capacitor. The load capacitor charges till it reaches the desired output. The capacitors used to transfer the charge from the source to load capacitor are known as charge transfer capacitors. These converters provide good efficiency at relatively light loads for conversion ratios close to the specific ratios provided by the topological combination used and are also favorable in terms of area. Stability and transient response depend on proper design of the power stage and controller. An efficiency curve of a switched converter reported is shown in Figure1.5a

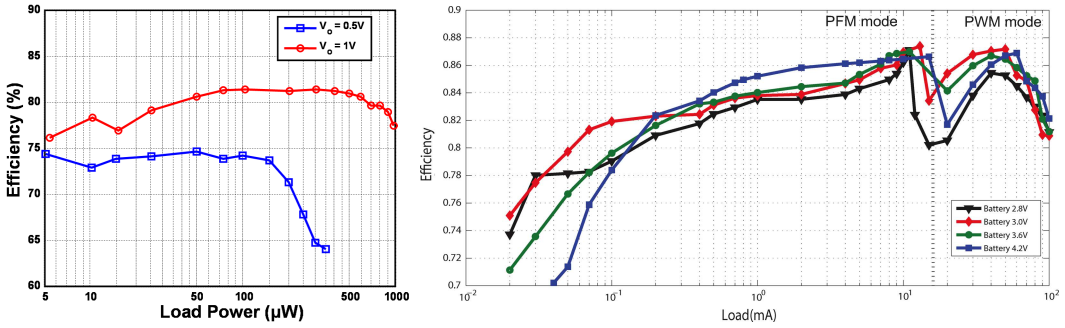


Figure 1.5: (a) Efficiency curve of SC Converter vs. Load Power [8] (b) Efficiency for Inductive Converter vs. Load Current [5]

Inductive converters utilize both inductors and capacitors, in addition to switches. A simple way to understand the operation of these converters is that the inductors and capacitors provide filtering for a switched signal (generated by switches) to extract its average (DC component) and reject the rest of the harmonics. The simplest buck converter consists of high side switch connected to source, low side switch connected to ground and an inductor or capacitor. Time is divided into periodic intervals. In each interval, the high side switch is switched on for some portion (D) of the period while the low side switch is switched for the rest ($1 - D$). The average value of the signal is DV_{in}. In addition, harmonics are found at multiples of $f = 1/T$. Connecting an LC filter will produce the average value plus some ripple. More complex filters and topologies are possible, but in integrated implementations size is extremely important and more often than not the simplest filter is used. Regulation is provided by connecting some negative feedback loop around the simple converter to control time intervals for which the switches are turned on and off. To ensure unconditional stability some form of compensation or control is required. These converters provide good efficiency at relatively heavy loads, require careful design to avoid area issues, and also some design effort for stabilization and obtaining good transient response. An efficiency curve of an inductive converter reported in the literature is shown in Figure1.5b

Notice in Figure1.5 that Switched Capacitor converter and Inductive Converter show good performance in different areas of loading. There is a possibility of obtaining wider range output if these two types of converters are merged such that each serves

the area of load where it performs best.

1.3 Main Blocks of DC-DC Converters

There are four main building blocks of a regulated DC-DC Converter: power stage, output sensing block, the controller and the drivers Figure1.6. The power stage has been discussed in previous section. The controller provides the control signal require to regulate the output based on information collected through the sensing block. The control action is executed on the power stage by the drivers.

Usually the output voltage is the most important signal since it is the quantity to be regulated. Instead of sensing it, it is more common to sense the difference between the reference voltage and the output voltage, commonly referred to as the error signal. This is usually amplified to a level suitable for processing, by an amplifier. Of course if the controller is digital then an Analog to Digital Converter is needed. The controller attempts to achieve the control objective of zero error signal. Controllers may also have secondary objectives for example to minimize ripple.

These blocks need not be separate. In the simplified description of LDO above the three blocks: sensing, controller and driver are all merged in one block. For switching converters however they are usually separate blocks. For example large switches in inductive converters are driven a driver block composed of inverter chains to reduce the turn on and off times for the switches.

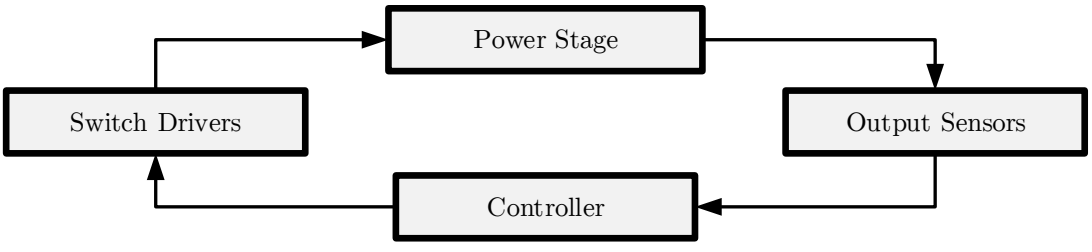


Figure 1.6: Main Blocks of a Power Converter

1.4 Research Objectives

Modern digital circuitry in portable applications demand efficient power converters that can be incorporated with the rest of the system or circuitry on the same chip. Efficiency is particularly important at light load since the circuitry spends a considerable amount of time in light load. Further techniques used to reduce energy consumption such DVS will have reduced effectiveness with reduced light load performance. Full integration on chip reduces system cost and footprint. Our objective is thus:

> *To design a power converter with improved efficiency over a wide range of loading conditions with full integration. The basic idea is to merge a switched capacitor converter with inductive buck converter to take advantage of their good efficiency in light load and high load respectively. A secondary objective is to reduce the impact of the merger on the area and other desirable characteristics by proper design of the controllers.*

1.5 Thesis Organization

Chapter 2 provides some of the necessary background for DC-DC converters and some of the main power stage converter topologies. Chapter 3 presents an algorithm that can used to analyze DC-DC converters. Chapter 4 describes the design of the switched capacitor converter. Chapter 5 discusses the design of the inductive converter. Chapter 6 discusses the merger of the two converters. Appendices A and B discuss the layout and chip test plan.

1.6 Thesis Contributions

1. This work presented a new algorithm that can generate the state space model representation of a power converter (sections 3.1 and 3.2). Further this work presented algorithms that allow the evaluation of, efficiency, ripple and output impedance from the state space representation (section 3.3.1)

2. This work proposed a Rail to Rail Multiphase Supply Independent Oscillator (section 4.4)

3. This work proposed a Hybrid Converter to enhance the loading range

CHAPTER 2

LITERATURE REVIEW

Switching power converters are defined as: converters utilizing switches and reactive elements (capacitors and inductors) to achieve power conversion [9]. This chapter presents a survey of the literature on this topic. Ideally the reactive elements are lossless elements and as such the conversions is lossless. Practically this is not the case. We will start by giving the mathematical definitions of several performance parameters. Next, the main loss mechanisms and their relation to the operating conditions of the converter. Next we discuss the converter power stage topologies, which is how the three types of elements are interconnected. In particular we are interested in topologies that will satisfy the same performance requirements while using less area. Next we discuss how various control techniques for converters. To completely specify a control technique we need to specify what inputs it needs and how it converts these inputs into control action. In the case of switching converters is mainly the timing of switches. We then discuss various power stage optimizations grouped along the three types of elements: switches, inductors and capacitors. Next we present techniques for acquisition of state information, which is used as the input to the controller and how the switches are driven by the controller. Finally we discuss some practical considerations to which attention must be paid during converter design.

2.1 Definition of Performance Parameters

With reference to the terminal definitions of a generic DC-DC converter as shown in Figure2.1 and assuming the interval $[T_1, T_2]$ to be after the converter has been running for long time i.e. at steady state

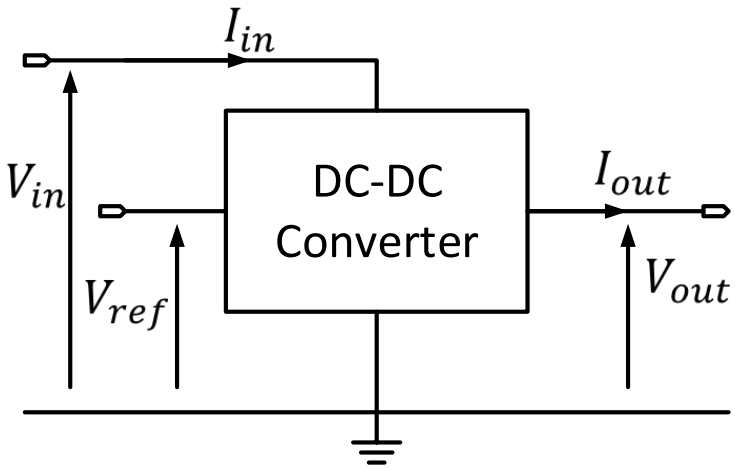


Figure 2.1: Generic Terminal model of DC-DC Converter

Efficiency

Efficiency is defined as energy output by energy input, given by the formulae:

$$\begin{aligned} \eta &= \int_{T_1}^{T_2} \frac{V_{out} I_{out}}{V_{in} I_{in}} dt \\ \eta &= \frac{V_{out} \bar{I}_{out}}{V_{in} \bar{I}_{in}} \end{aligned} \tag{2.1}$$

Efficiency is an important parameter for a DC-DC converter, especially is power constrained low power applications.

Ripple

Ripple Voltage is defined by:

$$V_{Ripp} = \max_{[T_1,T_2]}(V_{out}) - \min_{[T_1,T_2]}(V_{out}) \tag{2.2}$$

Ripple given an indication of how noisy the converter output is. For digital loads ripple corresponds to unusable voltage headroom since timings are all based on the minimum voltage. As such it also contributes to energy loss [10].

Output Regulation

Output regulation defines how at steady a change in load or input voltage causes a change in the output. The load regulation is defined by:

$$R = \Delta V_{out} / \Delta I_{out} \tag{2.3}$$

It can be seen clearly that the units are of an impedance.

Transient Response

The transient response indicates the time required by the converter to regulate the output voltage back to the reference voltage after a transient in the load, reference or input voltage is applied. This is usually defined by the settling time of the converter. Assuming the transient evenbt occurs at $t = 0$, the settling time is defined as:

$$T_{settle} := \{T : |V_{out}(t) - V_{ref}| < \alpha V_{ref}\} \qquad \forall t > T \tag{2.4}$$

For sampled data (from a digital oscilloscope or simulation) the definitions in [11] can be used. Instead of stating the settling time a maximum rate of change can be stated. For example 20mA/ns indicates that it can regulate load changes at such a rate (as long as the final and initial values are within the loading range of the converter).

2.2 Main Loss Mechanisms

2.2.1 Conduction Loss

Conduction is loss due to current flow in the power stage. Elements of the power stage whether they be inductors, capacitors or switches (transistors) have some loss.

To first order this can always be modelled by an equivalent resistance in series with an ideal element. In the case of the switches this is important in the ON state of the switch, in which case it is called the on resistance. For the inductor it is called DC Resistance (DCR) of the inductor. For the capacitors it is called Equivalent Series Resistance (ESR). In any case the loss power dissipated in such an element is given by:

$$P_{cond} = I_{rms}^2 R_{eq} \tag{2.5}$$

To reduce this form of loss one either has to reduce the root mean square current I_rms or the equivalent resistance R_eq. Note that on-chip passive components are usually known for their bad quality and hence relatively high R_eq. For switches this can be controlled by increasing the width and always using minimum length transistors. Further, this loss mechanism scales with the load current. The higher the load the higher the conduction loss and vice versa. As such it does not limit light load performance.

2.2.2 Switching Loss

Switching the transistors of the power stage ON and OFF every cycle requires charging the gate capacitance and discharging it every cycle. Since this is usually done through a resistive driving circuit, there is a loss. This loss is given by the well-known formula:

$$P_{sw} = C\Delta V^2 f_{sw} = C_{ox} W_{eff} \Delta V^2 f_{sw} \tag{2.6}$$

W_eff is the effective width of the transistor, ΔV is the voltage change between the two states of the gate voltage, f_{sw} is the switching frequency of that transistor and C_{ox} is the oxide capacitance per unit width at the minimum length. Note that this loss mechanism to a first order has no dependence on the load current. As such it is one of the limiting mechanisms at light loads where it becomes a dominant loss. Although we have discussed this in the context of switching transistors, any node that changes voltage levels periodically will have a similar loss. This usually due to

parasitic capacitances at that node. In such a case a similar formula applies.

2.2.3 Shoot Through Loss

If any switches are on and form a connection between the input supply and ground, a relatively large current may flow. This current is known as Shoot Through current and will cause a large dissipation of energy. Further if this event repeats periodically the loss will be further exacerbated. This issue is avoided by adding a dead time to the switching signals of transistors which occupy a path from input supply to ground. The dead time must be such that it gives transistors time to switch off but not large to disturb the operation of the rest of the circuit. The loss can be estimated as:

$$P_{ST} = V_{IN} I_{STRMS} \tag{2.7}$$

To a first order this is independent of load current and if not designed for will limit light load efficiency.

2.2.4 Control Circuitry Loss

Control circuitry generates the control signals for the power stage. The exact power loss will of course depend on the control scheme used. In many control schemes this can be considered a constant. This again implies that as load decreases efficiency decreases and hence light load efficiency will decrease. Hence efficiency can be expressed as:

$$\eta = \frac{P_{Load}}{P_{Load} + P_{cond} + P_{SW} + P_{ST} + P_{CTRL}} = 1 - \left(\frac{P_{Loss}}{P_{IN}}\right) \tag{2.8}$$

where: $P_{Loss} = P_{cond} + P_{SW} + P_{ST} + P_{CTRL}$ and $P_{IN} = P_{Loss} + P_{Load}$

2.3 Inductive Converter Power Stage Topologies

2.3.1 Basic Buck Converter Topology

The basic buck converter topology is the most commonly used amongst the inductive topologies. It is shown in Figure2.2a. It consists if a high side switch (MP), a low

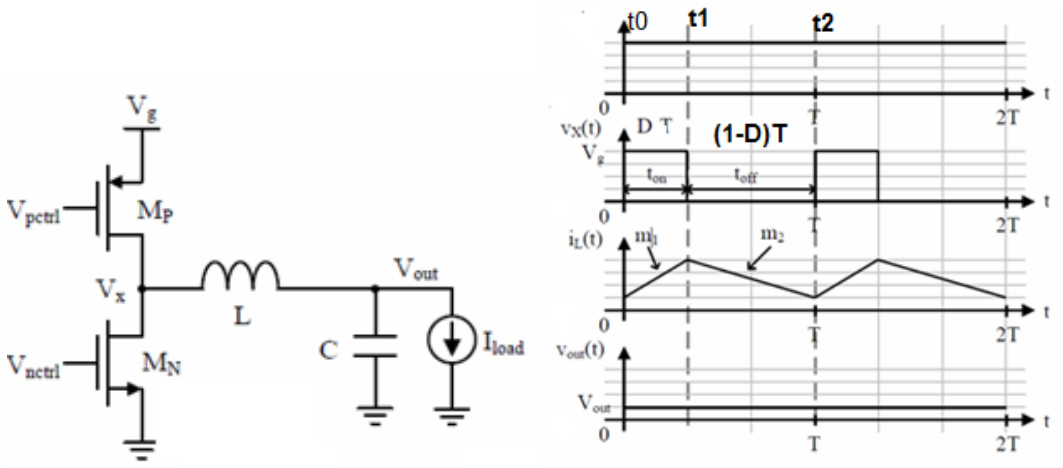


Figure 2.2: Basic Buck Converter (a) Topology (b) Important signals waveform shape.

side switch (MN) and an output LC filter composed of a capacitor and inductor. A basic understanding is that switching produces a signal with some duty cycle D at the node V_X. The LC filter then produces a filtered version with all harmonic except the DC components greatly attenuated. The appearing DC component has a value of DV_{in} and as such the output voltage can be controlled by varying the D. A more detailed analysis is as follows: assume the converter is well designed and operates in steady state such that the output voltage is almost constant. Also assume that the switches are ideal. The waveforms of the important signals are shown in Figure2.2(b). At time t_0 V_X is connected to V_{IN} through MP. Since V_X is fixed to V_{IN} the inductor voltage $V_L = V_{IN} - V_{DC}$ is also a constant and hence the inductor current ramps up almost linearly till time point $t_1 = DT$. At that point MP is disconnected and MN is connected. The inductor current ramps down till the end of the cycle at $t_2 = t_0 + T$. Since steady state is periodic by definition then $i_L(t_0 + T) = i_L(t_0)$ and one can also deduce that the current delivered to the load is the average of the inductor current.

Notice the waveforms in Figure 2.2(b) are idealized assuming large capacitor to make the ripple very small. In fact, a real converter will never have zero ripple at the output. The ripple at the output can be decomposed into two components: capacitive formed over output capacitor and resistive formed across the ESR.

2.3.2 Simple Buck Converter with Flying Capacitor

The flying capacitor topology is very similar to a simple Buck Converter. The addition is the "flying capacitor" C_{FLY} between the input voltage and output voltage as shown in Figure 2.3(a). Notice that the diagram adds the equivalent series resistance of each element. There are two reasons for adding this capacitor: ripple cancellation at the output and reduction of the input decoupling capacitor value [12]. In Ref. the authors analyze the simple buck converter and claim that ripple signals at V_{IN} and V_{out} are close to 180 degrees out of phase which provides good opportunity for ripple cancellation. The signals are shown in Figure 2.3(b). The simulated attenuation of ripples from the aforementioned reference are shown in Figure 2.4 The authors did not report what definition of ripple attenuation was employed by the authors.

It is important to notice that the input ripple is usually minor; however at high frequencies the bondwire parasitic inductance at the V_{IN} IC connection resonates with the input decoupling capacitor at a frequency that might be close to the switching frequency. In such a case there might be excessive ripple that damages the performance of the converter. C_I needs to be increased to move the operation to the flatter side of the LC resonance curve. This however incurs additional area. Another option is to attempt to reduce the ripple which can be done by employing the flying capacitor as done in this topology by the authors of [12].

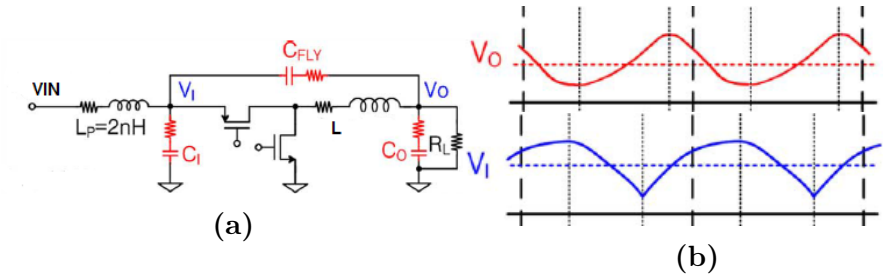


Figure 2.3: Flying Capacitor Buck Converter (a) Topology (b) Waveform of Input and Output Voltages with 180 phase shift [12]

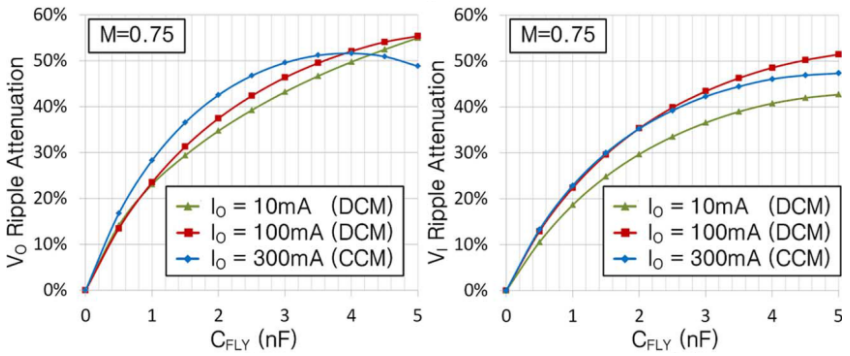
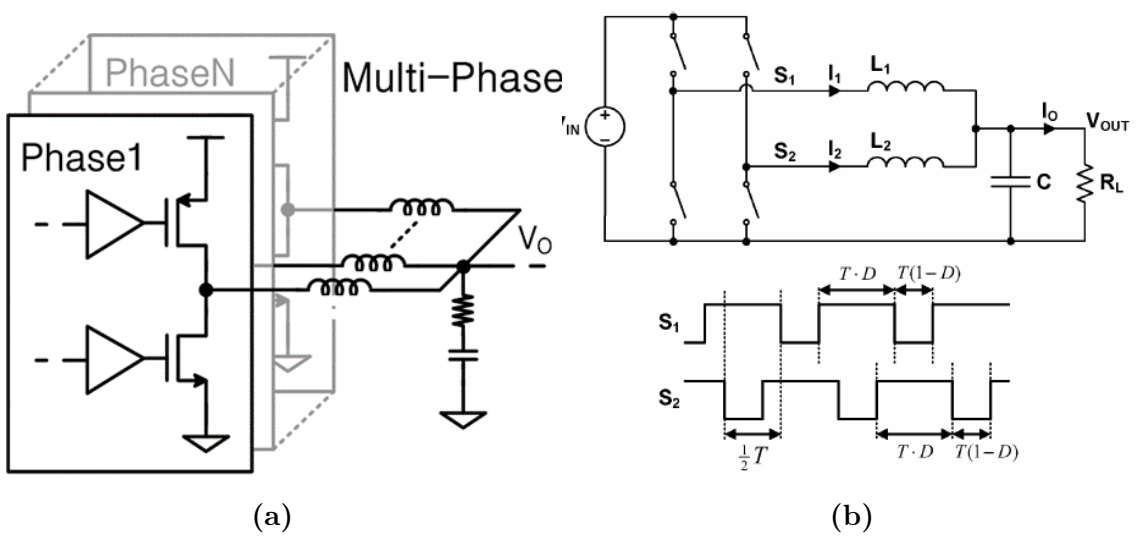


Figure 2.4: Ripple attenuation at input and output nodes for varying flying capacitor values [12].

2.3.3 Standard Interleaved

This topology is a parallel connection of N identical copies of another simpler topology as shown in Figure 2.5(a). 2.5(b) shows a two phase standard interleaved topology formed from two simple buck converters. Note that the output capacitors can be replaced by one capacitor, since they are in parallel. The identical copies are not driven by in phase signals. Rather, the driving signals of each phase are shifted out of phase by $360/N$ where N is the number of interleaved phases. This technique is relatively common in the recent literature, [12–14].



(a) **(b)**

Figure 2.5: Standard Interleaved Topology (also named Multiphase) (a) a generic diagram [12] (b) for N = 2 case. [15]

Some of the reasons for using this topology are: reduction of ripple, reduction of output capacitor size and adaptive sizing of the power stage. The reduction in ripple comes from the fact that the ripple in the different phases is ideally identical and out of phase by $360/N$. These ripple currents add at the output node. At duty ratios which correspond to integral multiples of this phase shift, complete cancellation of ripple can be achieved. Duty ratios in between achieve less ripple attenuation, [12]. Figure 2.6 shows normalized ripple amplitude for interleaved topologies with N = 1, 2 and 4 as it varies with duty ratio. For the same output ripple amplitude, the output capacitor can be reduced in size since the ripple at the output has a frequency N times higher than the switching frequency f_{SW}. Finally adaptive sizing of the power stage is a useful technique to cope with various loads. The basic principle is that at light loads not all the phases are used instead some are turned off. This reduces the effective width and hence the switching loss. A good example of how adaptive phasing is used with a combination of other adaptive techniques can be found in [12, 14].

The above discussion has assumed that the designer is able to obtain identical copies of the unit topology. However variability of manufacturing processes needs a more robust design technique. In [12] Average Current Balancing Calibration loops are proposed that even out the current carried by the interleaved phases even under process variation.

Issues with using an interleaved topology are the stringent timing requirements. Each phase must be shifted from the other by $360/N$. For a $100MHz$ frequency this is already $2.5ns$ which is a relatively small interval. The usage of Phase Lock Loops to guarantee this phasing requires area and consumes power. Powers of two can be generated digitally with relative ease. Further, there is extra area required in the controller, and driving stage. For inductive converters it might be difficult to fit more than one inductor on an IC and this will require accounting for mutual inductance. Ref [12] utilizes off die but on package bondwire inductors to avoid utilizing large area on chip and reducing the effect of mutual inductance on the performance.

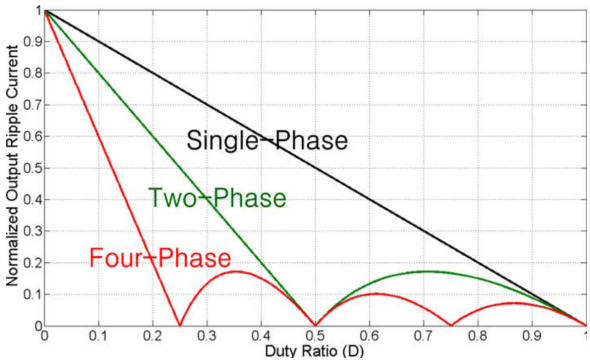


Figure 2.6: Normalized ripple amplitudes for a standard interleaved topology with N = 1, 2 and 4 [12]

2.3.4 Stacked Interleaved

In this topology two phases of the simple buck topology are used. One is a primary phase and the other is the secondary phase. As shown in Figure 2.7, the secondary phase is driven by inverted signals with respect to the primary phase. In principle this generates ripple that is exactly out of phase with that of the primary. Ripple cancellation can be achieved if these two ripple currents are added at the output. To avoid DC loading of the secondary by the primary a capacitor CS blocks the DC. At steady state no DC current flows between the two phases. The ripple however is an AC signal and will flow, In short we generate a ripple signal and use it to cancel the primary phases ripple. Ideally the cancellation is complete however, non-idealities and parasitic do not allow complete cancellation. Monolithic implementation of this topology requires using two inductors, since they are in close proximity there is a certain mutual inductance between the inductors LP and LS. This can hinder or improve ripple cancellation. It can also decrease or increase the effective value of the primary inductor. In [15] the authors propose this topology, provide an analysis and shows that the mutual inductance can be used to improve effective inductance and reduce ripple for a wide range of duty ratios. The effect of varying the mutual coupling on the overall system efficiency is shown in Figure 2.8 (dark black like). The is driven by one signal using only inverters since the phases are supposed to be 180 degrees out of phase. This is in contrast to standard interleaved topology which requires precise phase shifting of the driving signals. As such one can assume that timing is much

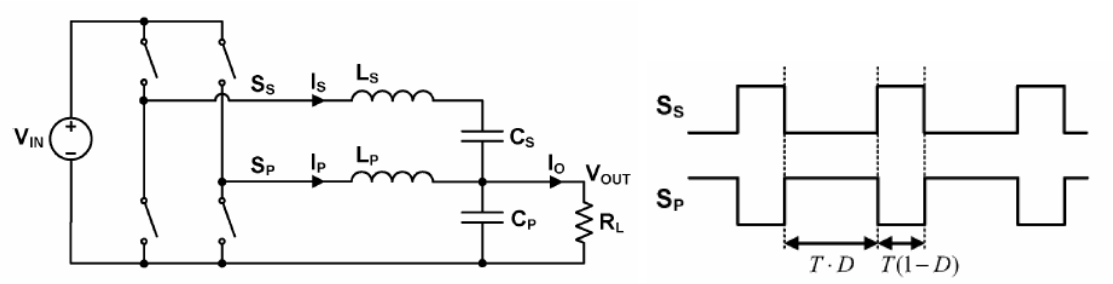


Figure 2.7: Stacked Interleaved Topology (a) Topology Circuit (b) Timing of primary and secondary phases [15]

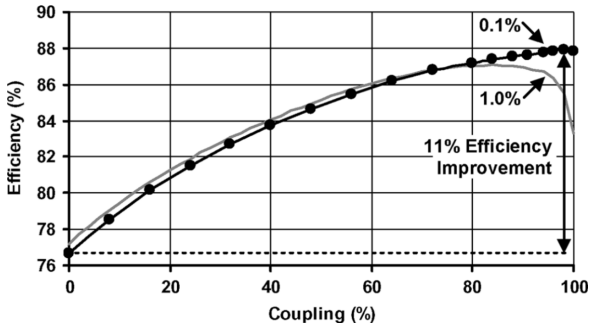


Figure 2.8: Effect of mutual coupling on converter efficiency [15]

closer to ideal in this topology. The effect of 1% phase shift due to timing mismatch on efficiency is shown in Figure 2.8. (Light grey line).

2.3.5 Three Level Converters

This topology is a merger between switched capacitor and inductive converters. It is shown in Figure 2.9. The topology attempts to reduce ripple at the output by reducing the voltage swing at node V_X. Rather than switching between VIN and GND every cycle the node switches between V_{IN} and $V_{IN}/2$ or $V_{IN}/2$ and GND. The reduction in ripple translate to smaller inductor for the same ripple size. The intermediate voltage is provides by C_{FLY} and a proper timing sequence of the switches. Compared to switched capacitor converters this topology provides better efficiency while utilizing more area. Compared to inductive converters it provides less ripple. [14]. However the driving of the switches is more complicated and required level shifting for the upper transistors. In fact the middle two transistors require two stages of level shifting. A

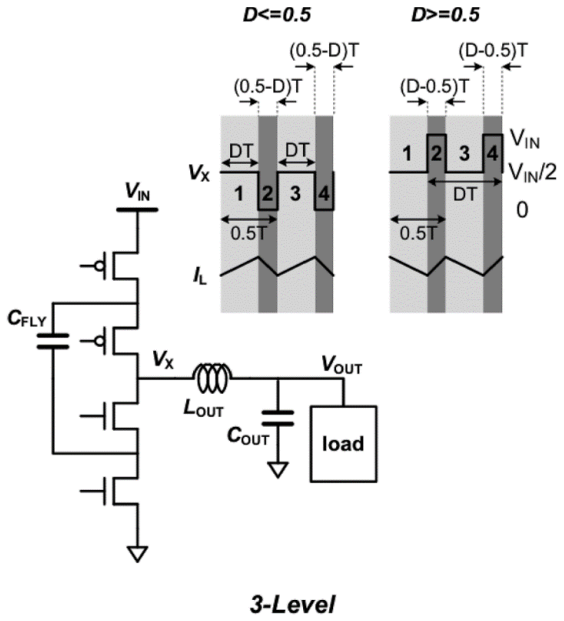


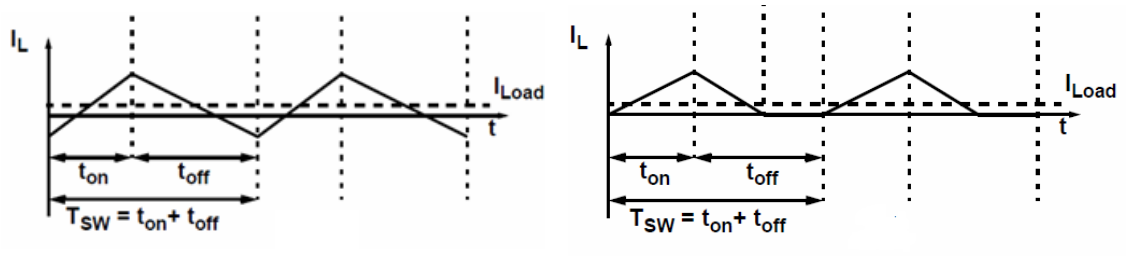
Figure 2.9: Three Level Converter Topology and Node V_X Voltage Level [14]

positive side effect is the reduced blocking voltages required by the switches [14].

2.4 Operation Timing and Control Techniques

2.4.1 PWM CCM vs. PWM DCM

Consider a simple buck converter. A Pulse Width Modulation (PWM) Controller in Continuous Conduction Mode (CCM) will close the High Switch (HS) for $t_{on} = DT$ time then will open the HS switch and close the LS switch for $t_{off} = (1 - D)T$ time. The output voltage assuming ideal switches is given by $V_{out} = DV_{in}$. To perform regulation the value of D varies with the error between the reference voltage and output voltage. If the voltage goes lower hence negative error D is increased and vice versa. To ensure stability there are requirements on the controller. First its output control signal D must be much slower than the switching frequency. This translates into the requirement that the feedback loop contain a compensator with limited bandwidth. Then normal analysis methods can be applied to find the pole locations and compensator designed such that the second of these has a gain of less



(a) **(b)**

Figure 2.10: PWM inductor current waveforms (a) CCM with $I_{Load} < \Delta i_L$ (Ripple) current. (b) DCM Waveform of inductor current.

than 0dB. This scheme is a very well-known scheme and has been thoroughly analyzed in the literature. Expression for some characteristics of this scheme are:

$$\text{Output Votage :} \quad V_{out} = DV_{in} \tag{2.9}$$

$$\text{Inductor Current Ripple :} \quad \Delta i = \frac{V_{out}(1-D)}{Lf_{SW}} \tag{2.10}$$

$$\text{Output Voltage Ripple :} \quad \Delta v_{out} = \frac{V_{out}(1-D)}{8f_{SW}^2 LC} \tag{2.11}$$

We notice that the inductor ripple to a first approximation appears to not depend on load current. As the load current decreases the ripple might exceed the load and hence we have negative inductor current. This means that the inductor is discharging the output capacitor and dissipating its energy to ground. This is a source of power loss and efficiency reduction. Discontinuous Conduction Mode or diode emulation mode attempts to remedy the negative inductor current that discharges the output capacitor by shutting off the low side switch. Instead of the waveform of Figure. 2.10(a) the inductor current looks as in Figure. 2.10(b). The controller detects (or estimates) the zero current instant of the inductor and issues a turn off signal for the LS switch. Too early switching off of the LS switch will cause a kick-back voltage from the inductor which will cause a dissipative flow through the body diode of the LS switch. The zero current point can be detected through circuitry sensing the inductor current or through the node VX's voltage.

At high frequencies with small inductor values (as is common in monolithic implementations), the detection of zero current point is not simple and the time available

to take action is also small. In [12, 16, 17] the authors describe a calibration loop that provides estimates that are improved every cycle based on the node VX's voltage of the previous cycles. They describe this as precise DCM operation and show that at steady state the calibration loop will eventually converge to the optimal turnoff time.

2.4.2 PWM vs. PFM

In PWM the switching loss is independent of load. As load decreases so does the efficiency. If the switching frequency is modulated with the load current then we can reduce the switching loss as load decreases. This is the basic idea behind Pulse Frequency Modulation (PFM). Since we will be varying the period. Duty ratio loses its meaning as a control variable. In the literature PFM methods either employ Constant On time or Constant Off time. Consider PFM scheme with constant on time: the controller senses the output voltage and when it falls below a certain level it issues a fixed width turn on signal for the HS switch. The inductor current ramps up. Then the LS switch is turned on after the constant on time has passed and the HS is switched off. When the current reaches zero the LS switch is turned off. Then the converters remains freewheeling for some interval till the output voltage falls below a specific threshold, where the process repeats. For heavier load this process repeats more frequently since output capacitor is discharged faster, while for higher load this happens less frequenctly. Notice that at steady state PFM and PWM-DCM are indistinguishable from the power stage waveforms and hence similar efficiency analysis apply after taking frequency into account.

2.4.3 Hysteretic Control

The hysteretic scheme dispenses with external timing mechanisms like clocks or ramp signals. In this scheme the controller compares the output to two threshold levels VH and VL. If the output exceeds VH then the LS switch is turned on. If the output is less than VL then HS is turned on. What is hoped is that charge is added or removed from output capacitor on a per need basis to keep it between limits. Notice that

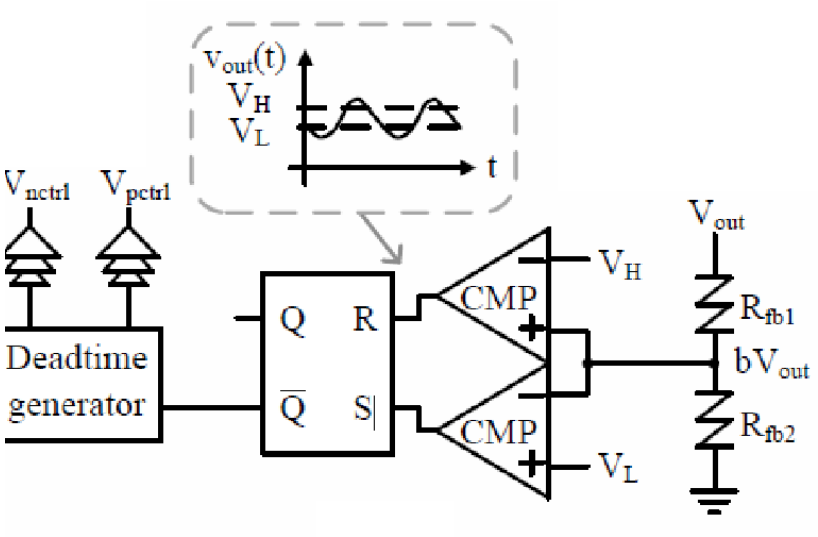


Figure 2.11: Hysteretic Controller and waveform of output [19]

frequency scales with load which means that switching loss scales accordingly. One might naively assume that the output ripple is bounded between VH and VL. This is not the case however. In [18] and [19] the authors show that any finite delay in the comparators, switching of MOSFETs or current resisting property of the inductor causes to ripple larger than VH – VL. This scheme also invalidates the assumption of linear ramp up and ramp down of inductor current. Since the period of switching is difficult to predict the analysis is more complicated. In [20] the authors provide an analysis technique for hysteretic controlled buck converters based on Charge Balance Analysis. A special case of hysteretic controller is when VH = VL. This is known as Single Bound Hysteretic Control. Hysteretic controllers have several advantages including unconditional stability by construction, and simplicity of controller. The unpredictability of ripple frequency render it unsuitable for interference prone applications. An extensive study of hysteretic controller is provided in [19]. Hysteretic converters were amongst the earliest switching converters to be fully integrated. [13].

2.4.4 Voltage Control vs. Current Control

In the schemes mentioned so far the sole control variable was output voltage. Control can also be achived by comparing the inductor current to reference currenti_C. The

reference current is generated by a compensator for the error signal of the output voltage. This dual loop systems is shown in Figure 2.12. When this loop settles down inductor current is proportional to the compensator output and $V_{ref} = V_{out}$. This technique has also been gaining some attention within the literature, [21–25]. There are several sub types: average current control, peak current control, valley current control. These schemes lend themselves easily to digitization with requirement of only one switching cycle as processing time. [22].

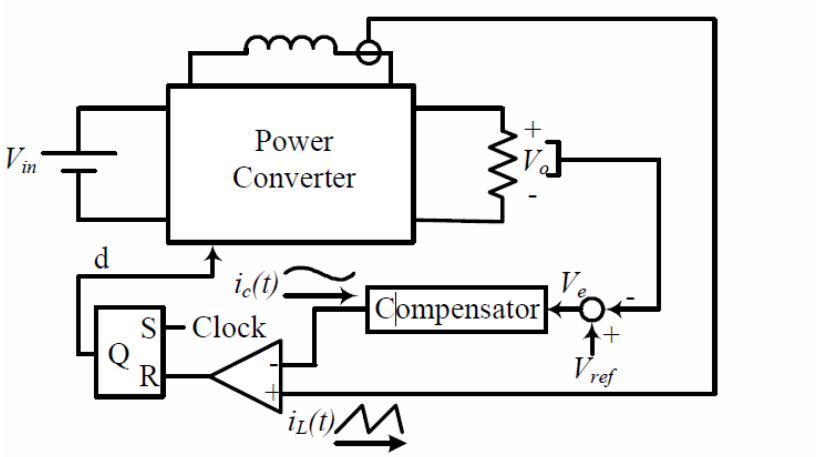


Figure 2.12: Current Mode Control showing extra inner loop [22]

2.4.5 Multi-Mode and Hybrid Mode Controllers

Controllers can merge than one scheme to take advantage of the merits of each. One common example is PWM/PFM mode hopping. PFM has good efficiency at light load while PWM has good efficiency at heavy load. Merging these two allows the controller to take advantage of both modes. In the simplest form, the designer decides on a threshold level of load current below which it is advantageous to switch to PFM. This method has been used in [5]. In some designs this can be made through external control. To make this fully automated there are a few issues the designer has to resolve: which mode of operation does the controller start in, how to avoid limit cycling between two modes if the current is close to threshold and stability of each mode. Allowing the controller to take these decisions can be implemented through a

finite state machine as in [26, 27]. In [28] the authors a controller switching between three modes based on loading conditions. The three modes are: PFM, PWM and dithering skip modulation (DSM). The DSM mode can be considered as a gradual change mode between PFM and PWM.

2.4.6 Digital vs. Analog Control

The schemes we discussed were all analogue in nature. They can also be implemented by digital controllers. Digital controllers for switching power converters were proposed in [29]. Since then they have seen much development as can be seen in [6]. The perceived advantages of digital controllers are flexibility and programmability, resilience to noise and aging. Also small area and power consumption especially as CMOS technology has scaled down and is heavily optimized for digital circuits. Finally there is the possibility of using more advanced algorithms. There are also disadvantages of digital controllers: such as requiring ADCs and DACs to convert state information and control commands to and from digital domain. Also techniques which are simple in the analog domain such as PWM are not so simple in the digital domain. There is a possibility of limit cycling if ADC resolution is insufficient. Digital controllers are under heavy research and improving. Ways to reduce power and number of ADCs are discussed in [27, 30]. A way to improve PWM DAC conversion is proposed in [5]. Advanced digital schemes are shown in [6, 31, 32]. Resolving limit cycles is discussed in [33, 34]

2.5 Switched Capacitor Converter Topologies

This section presents a brief discussion of the second type of switching converters: switched capacitor converters. They are also given the name charge pumps in the literature. They have come under heavy research recently. In [35] the authors from their literature survey conclude that SC converters can support more power density (output power /per unit area) than inductive converters.

We will first discuss the principle of operation and some terminology related to

SC converters. Next we shall discuss techniques/topologies of combining the simpler topologies to improve performance or expand output conversion ratios. Unlike inductive converters, SC converters do not have an arbitrary output tuning range through a parameter like the duty ratio. Rather, the output is produced with highest efficiency at discrete ratios. Intermediate voltages can be generated by an effect similar to LDOs (output resistance modulation). We will discuss some control schemes used for SC converters. Many of the loss mechanisms and mitigation techniques are similar to those for inductive converters and will not be discussed here. One loss mechanism specific to SC converters is bottom plate parasitic loss.

2.5.1 Principle of Operation

Consider the circuit shown in the figure 2.13 [8]] The circuit is supplied from a battery VBAT and consists of two charge transfer capacitors CT, one load capacitor CL and associated switches. Switches marked with ϕ_1 switch in phase 1 and switches marked with ϕ_2 switch on in phase 2. In the first phase VBAT charges the two charge transfer capacitors to VBAT/2 each. In the second phase the capacitors are connected in parallel and applied across the load capacitor CL. This repeats many times. Eventually the capacitor CL reaches VBAT/2 and no more charge is extracted from VBAT. At this points the output voltage is VBAT/2 thus achieving voltage level conversion.

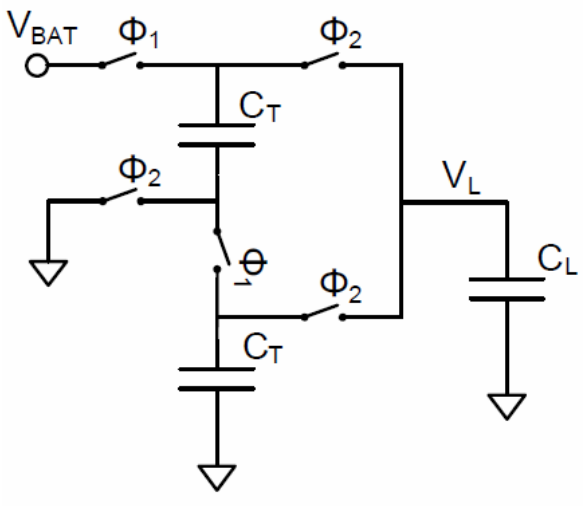


Figure 2.13: Switched Capacitor Converter with 1/2 Conversion Ratio [8]

2.5.2 Switched Capacitor Terminology

The terminology here is from [36]. As stated earlier SC converters are converters consisting of only capacitors and switches. In general they can have M-ports although we will restrict out discussion to two port NW. A converter may have several stages between the input and output. A stage can provide one or more conversion ratios under no load. By properly selecting the stage ratios many overall conversion ratios can be obtained. Each stage can consist of one or more identical topologies known as interleaved phases. A topology consists of a set of switches and capacitors. Each switch is activated during one or more time intervals known as clock phases. By switching the switches through the clock phases the converter performs the voltage level conversion.

The ratio between the input and output voltages under no load condition is the voltage conversion ratio. The voltage conversion ration can be obtained by inspection of the connections in the two phases. The analysis of switched capacitor circuits is more developed than inductive converters. [36] provides a general method to analyze a switched conversion circuit. One of the parameters produced by this analysis is the voltage conversion ratio under no load condition. It is important to that although SC Converters have discrete conversion ratios it does not mean they cannot regulate the output to some lower level. As shown in [36] the output voltage is given by:

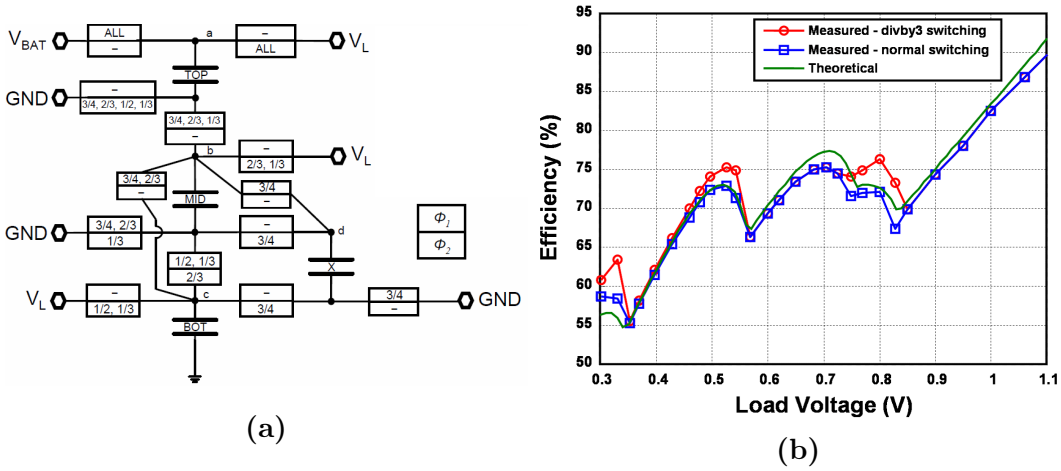
$$V_{OUT} = nV_{IN} - i_{OUT}R_{OUT}(f, D_i, G_i) \tag{2.12}$$

R_{Out} which depends on frequency and switch conductance, allows regulation of the output to some desired level at the cost of an efficiency loss.

2.5.3 Reconfigurable Topologies

The topology shown at the beginning of this chapter produce fixed ratio of 1/2. However for DVS applications several voltage levels are needed. In figure 2.14(a), a topology is shown that is capable of producing multiple conversion ratios. Each split box

represents a switch that closes in the conversion ratios noted in the box. If the ratio is noted in the upper half then it operates in phase 1 or phase 2 if it is noted in the lower box. The ratios are 1/1, 3/4, 2/3, 1/2, 1/3. Some ratios suffer more from the bottom plate capacitor loss and conduction losses and as such the efficiency varies considerably with ratios as shown in Fig. figure 2.14(b).



(a) (b)

Figure 2.14: (a) Reconfigurable topology from [8] (b) Plot of efficiency vs. output voltage

2.5.4 Topology Combination

There are two main techniques to combine SC converters. Cascading and Interleaving. Interleaving similar to interleaving in inductive converters utilizes identical topologies in parallel with phase shifted driving signals. Similar considerations apply when it comes to ripple reduction, output capacitor reduction and adaptive sizing. This technique has been used in several converters, [37].

The other technique is cascading stages and in this technique the stages don't have to be identical. In [36,38], the authors provide a technique for optimizing the cascade and finding its optimal ratios and efficiencies under different configuration. In [39] the authors show an 8 stage cascade to produce an output voltage tunable to 31mV. Of course this many stages harm efficiency and it stays below 70% throughout the load current range.

2.5.5 Enhanced Current Output Topologies

The topologies shown in figures 2.13 and 2.14 both charge the output during only one phase ϕ_2 and depend of on the output capacitor to supply the load in ϕ_1. This however is not the best utilization of the capacitors. A topology that is very commonly used in the literature [8, 10, 37, 40, 41]is shown in figure 2.15.

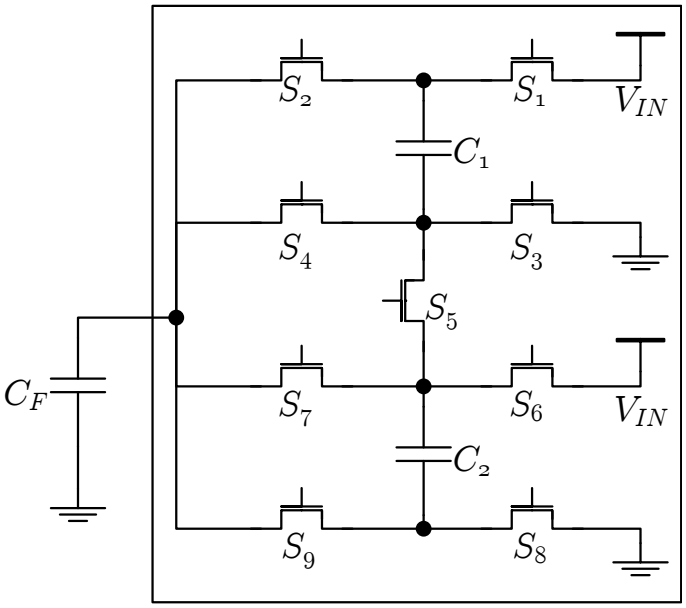


Figure 2.15: Topology that delivers output on both phases

2.5.6 Control of Switched Capacitor Converters

The relation between output voltage, input voltage and other parameters of SC converter operation is given by:

$$V_{OUT} = nV_{IN} - i_{OUT}R_{OUT}(f, D_i, G_i) \tag{2.13}$$

The three parameters allowing regulation are frequency f and the switch duty cycle D_i and switch conductance G_i. The ability to vary switch conductance is relatively limited to adaptive width sizing. The duty ratio is kept at 50% for minimum ripple. The only parameter that can vary over the orders of magnitude is the frequency. Traditional control methods relied on sensing the output voltage error and output

current, passing them through a compensator (for stability) and then using the result to control a voltage controlled oscillator (VCO). The two simplest methods for control are Hysteretic control methods and Pulse Skipping.

Similar to hysteretic control in inductive converters hysteretic methods as applied to SC converters employ comparators and upper and lower reference voltages VH and VL. The controller detects when these limits are passed and changes the state of the converter in the opposite direction. This method has several derivatives: lower bound hysteretic control [36], Single Bound Hysteretic Control (SBHC) [42, 43], adaptive double bound hysteretic control [44] and has been (to the best of my knowledge) the most common in SC converters.

Pulse Skipping also employs comparators to compares the output to the desired reference. The converter by default in ϕ_1. When the output falls below reference the controller switches to ϕ_2 and charge is transferred to the output capacitor. This raises the voltage. This is done repeatedly till the voltage exceeds the reference. This has been used in [8] for steady state control. In transients (detected by an overload comparator) a special frequency scaling system doubles the switching frequency and doubles the switch sizes repeatedly till converter is able to cope with the load.

2.6 Power Stage Designs/Optimizations

2.6.1 MOSFET Designs/Optimizations

Static Switch Sizing

There are two main loss mechanisms associated with MOSFET Switches: Conduction Loss due to source drain resistance and Switching Loss due to charging and discharging of the gate. The switching loss is proportional to the capacitance seen at the gate (including Miller effect capacitance), which is proportional to the width. The conduction for a given drain current is proportional to the resistance which is inversely

proportional to the width. As such this can be expressed as:

$$P = C_{eff} W V^2 f_{sw} + \frac{I_{rms}^2 R_0}{W} = aW + \frac{b}{W}$$
$$\frac{dP}{dW} = 0 \rightarrow W_{opt} = \sqrt{\frac{b}{a}}$$
$$\therefore \qquad W_{opt} = I_{rms} \sqrt{\frac{R_0}{C_{eff} W V^2 f_{sw}}} \tag{2.14}$$

Notice that the optimum width varies in terms of switch current (which depends on load current proportionally). This means that for smaller load currents we need smaller widths and vice versa. Also notice that since charge carrier mobility in P-MOSFET is lower than in N-MOSFET the width for NMOSFET will be smaller than that for a PMOSFET with similar loading conditions and technology.

Adaptive/Dynamic Switch Sizing

In static switch sizing the switch width is chosen at design time by the designer and optimized for some specific load. If it is optimized for light load then efficiency is reduced at heavy load and vice versa. Designers will usually optimize for maximum load since that ensures that the current carrying capacity of the MOSFET is not exceeded. This leads to suboptimal performance at light loads. A technique introduced in [45] and which became more common since [12, 14, 26, 46] is adaptive sizing of FETS. A controller measures the load current (through some sensing mechanism) and based on it decides the width of the FET to use. This ensures the MOSFET size is close to optimal even for variable loads. Hence with everything else not changed this provides a more constant efficiency over a wide load range. A more thorough analysis is in [47]. The scheme is shown in Figure 2.16 [46].

Stacked/Cascode Switches

In deep submicron processes the voltage blocking capacity of MOSFETs is not very large. For example the LF110nm process from L-Foundry has a maximum blocking voltage of 3.3V. To allow withstanding more voltage e.g. direct 4.2 battery connection

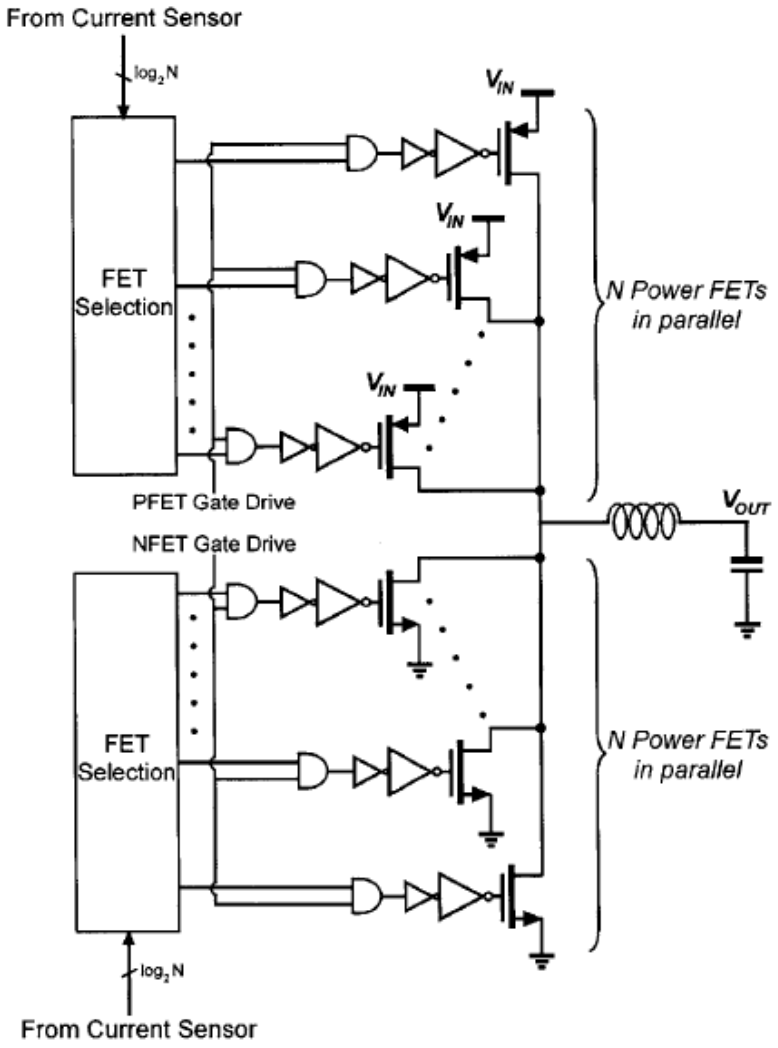
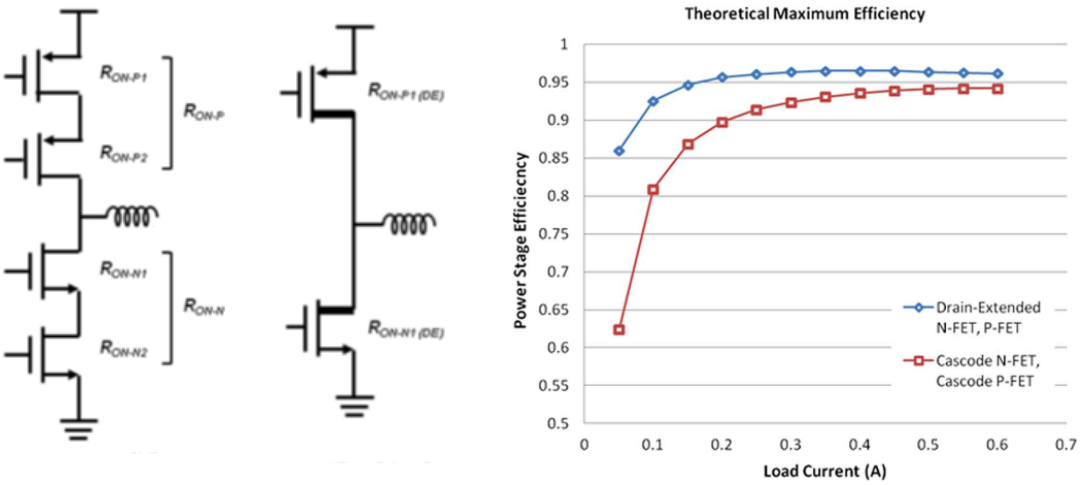


Figure 2.16: Adaptive FET Sizing Scheme [46]

the designer has to stack more transistors. The other option is to use Extended drain MOSFETs (next section). Although cascading doubles the voltage blocking capacity of the switch, it effectively increases the length and hence resistance. The conduction loss in the transistor doubles. Further, the driving circuitry becomes more complicated as each switch is referenced to a different voltage level. [5] Cascoded switches are shown in Figure 18(a).



(a) **(b)** **(c)**

Figure 2.17: (a) Cascode Switches (b) Extended Drain MOSFET (c) Efficiency Comparison for varying loads from Ref. [6]

Extended Drain Switches

Extended drain MOSFET are MOSFETs constructed with a light doping region before the actual drain. This gives a higher voltage standing capability for the MOSFET. This introduces a slightly larger resistance. Extended Drain MOSFETs (LDMOS) where introduced in [48]. Reference [6] provided a comparison between Cascoding and LDMOS and concludes that they are more efficient. This however is depends on technology. The advantage of using LDMOS is that no driving circuitry redesign is required. The same driving circuits that drive ordinary MOSFETS will work. The Miller capacitance between drain and gate of LDMOS is also lower than usual High threshold voltage transistors. The issue with LDMOS is that they are not available in every process or only one of them is e.g. N-LDMOS. [2]. The symbols of LDMOS as drawn in circuits are shown Figure 2.17(b). An efficiency comparison between cascoding and LDMOS for 45nm process is shown in Figure 2.17(c), [6].

All NMOS Switching

To obtain the same ON resistance from a PMOSFET as an NMOSFET a PMSOFET must occupy larger area since the holes carrier mobility is lower than electron mobility.

Thus if we can replace the PMOSFET with an NMOSFET one can reduce some area (or reduce power loss for the same area.). In [49] the authors propose an all NMOS switching scheme. They propose charge pump based drivers to drive the high side switch. The converter shows 2% increase in efficiency with a 2% reduction in area of the power stage.

2.6.2 Inductor Designs/Optimizations

Standard Spiral Inductor (Single/Multilayered)

This is the simplest and most straight forward way of implementing inductors on-chip. One or more metal layers are used and wound round in spiral shapes. This can produce inductance values in the Nano-Henry range for an areas in fractions of millimeters. The quality factors however are very low (less than 10). In fact a rough estimate for the resistance is a few hundreds of milliohms per nH. This has been used in several references, [14, 26, 50, 51]. A procedure for designing and optimizing such inductors is discussed in [52]. Using several layers in parallel can reduces the DCR of the inductor but increase its parasitic capacitance [53]. Increase capacitance will manifest as increased ripple and power loss.

Asymmetric Multilayer Inductor

In a buck converter there is little voltage variation on the output side hence increasing the capacitance on this side is not a big issue (note that this line of reasoning requires using a more complicated model than that we mentioned earlier, at least a pi model which allows for asymmetry of the two sides of an inductor). This allows us to use as many layers as possible on the output side to reduce resisatnce. The side close to the switching node VX is made with a reasonable number of layers to avoid excessively increasing the series resistance or increasing capacitance. This design was proposed in [54] and shown in Figure 2.18

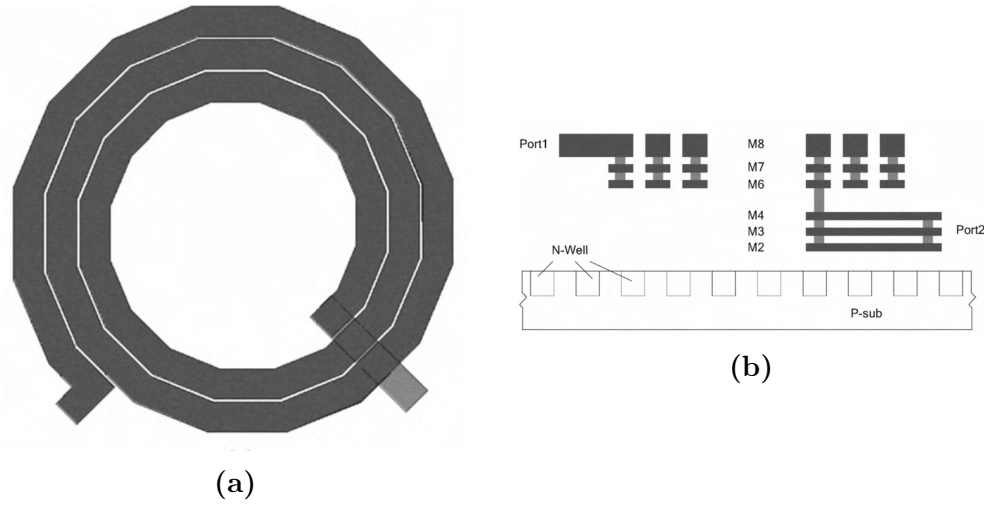


Figure 2.18: Asymmetric inductor (a) Top view and (b) cross sectional view [54]

Mutually Coupled Inductors

Any two conductors in close proximity will have a mutual inductance M. This is true for inductors. The mutual inductance between two inductors can make the effective inductance of one inductor look larger or smaller depending on the relative phase of the currents. [15] uses the mutual inductance of two inductors to increase the effective inductance of a primary phase in a stacked interleaved topology and effect ripple cancellation. A die photograph showing these inductors wound on top of each other is shown in Figure 2.19

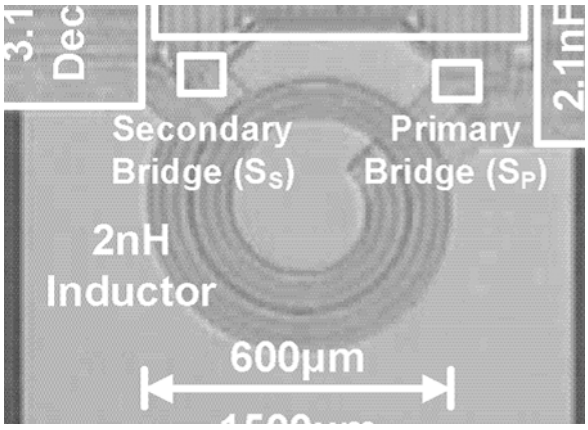


Figure 2.19: Die micrograph of two inductors wound into each other [15]

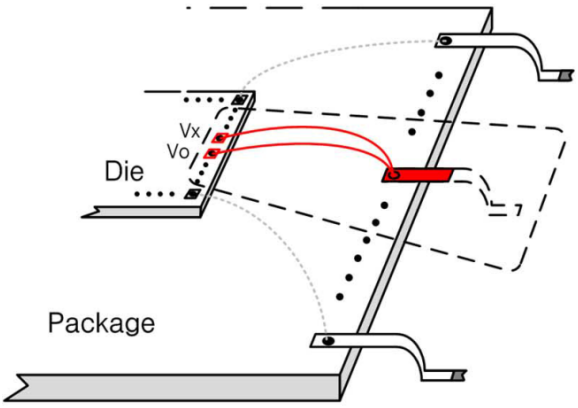


Figure 2.20: Bondwire inductor on package but off die [17].

Bondwire Inductors

Bondwire is the wire that connects pad on die to pins on chip. This wire being relatively long has some inductance and can be utilized as an inductor at high frequencies. This has been used in [12, 16, 49, 55] These inductors provide better inductance than on-chip spirals and lower series resistance. On the other hand they are prone to more variability since they are not part of die fabrication process. They can vary as much as 100% or more. In [16, 17] the authors propose a precise DCM calibration loop, that counters the effect of this variability when it comes to DCM operation. Bondwire and pads are shown in 2.20.

2.6.3 Capacitor Designs/Optimizations

MOS Capacitors

The gate oxide of a MOSFET can act as a capacitor when the other three terminals (Drain, Source and Bulk) are shorted together. In many processes due to the very small thickness of the oxide (tens of Angstroms) the MOS capacitor is provides the largest capacitance density. However the capacitance is nonlinear. This means that a MOS cap is used as the output capacitor of a buck converter then the ripple and DC signal see different capacitance values. This can complicate the analysis.

MIM Capacitors and MOM Capacitors

These employ additional insulator layers specifically placed between the metal layers to increase the capacitance. The metal upper metal layer is extended downwards to decrease the distance and increase capacitance. These are usually used placed in higher layers to reduce bottom layer parasitic. If the insulator is an oxide they are named MOM. If other insulators are used such as SiN or TaN then it is called MIM. The metal from the upper layer is "pinched" down to decrease distance and increase capacitance as shown in Figure 2.21

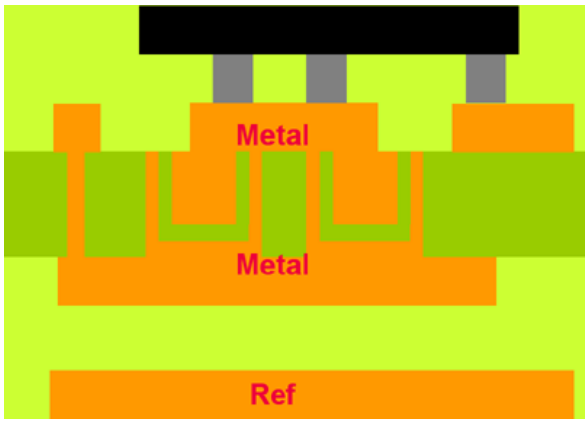


Figure 2.21: MIM Capacitor

Lateral Field Capacitors

Parallel plate capacitor discussed so far utilize vertical fields between one layer and the next. As technologies scale down lateral dimensions scale faster than vertical ones. Utilizing the shorter lateral distances can provide higher capacitance densities. This is thoroughly investigated in [56]. The authors conclude that lateral field capacitors can perform better than traditional parallel plate vertical field capacitors. Two of their designs: the Vertical parallel plates structure and Vertical bars structure are shown in Figure 2.22

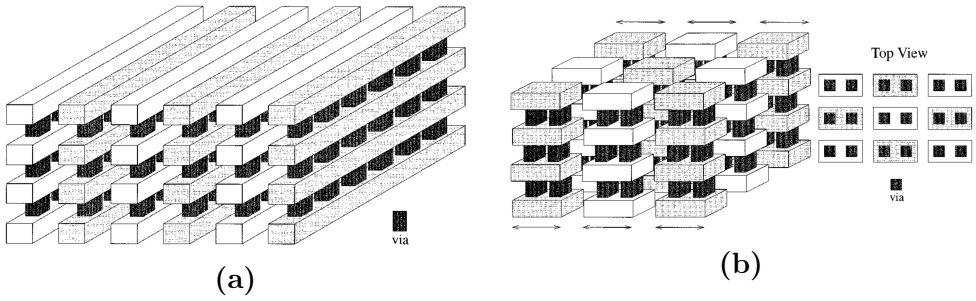


Figure 2.22: Lateral field capacitors (a) vertical parallel plates and (b) vertical bars structure [56]

2.7 Sensing Design

2.7.1 Output Voltage

To reduce the output voltage to a level usable by the active circuitry it a resistive feedback divider is usually used. This is then followed by an error amplifier. This can then be fed directly to the controller. For digital control an ADC is needed to digitize this signal. This circuit is shown in Figure 2.23

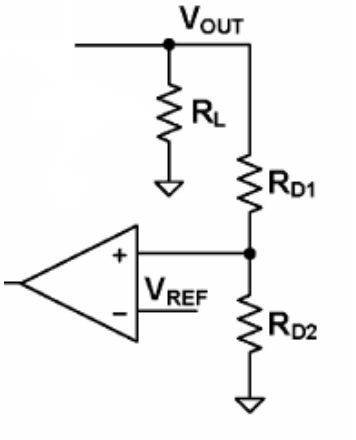


Figure 2.23: Output voltage sensing circuit

2.7.2 Inductor Current

Inductor current can be sensed by RC filtering the voltage across the inductor. Derivation of the relations are in [57]. The filter depeding on its connection can produce

either the inductor current as in Figure 2.24a or the average inductor current as in Figure 2.24(b). [57]

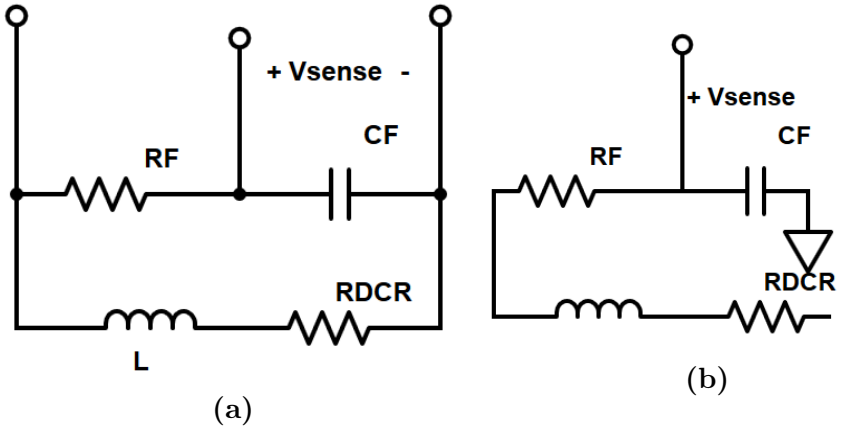


Figure 2.24: Inductor current sensing (a) filtering method (b) average current only [57]

2.7.3 MOSFET Switch Currents

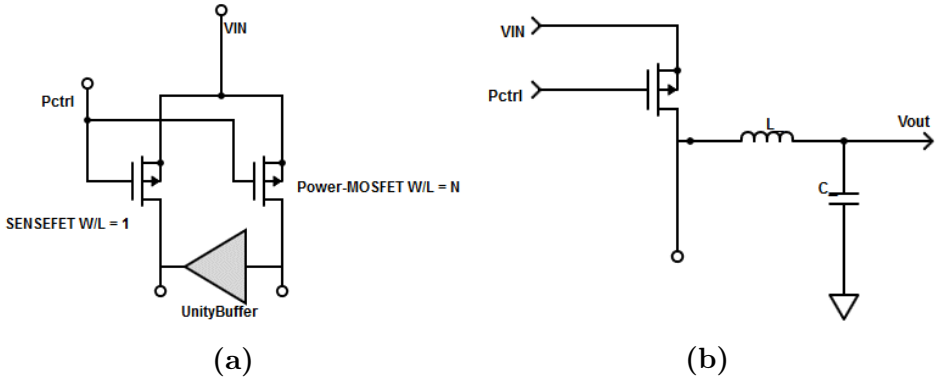


Figure 2.25: MOSFET Current Sensing (a) SENSEFET (b) RDS Sensing. [57]

The basic idea in SenseFETs is to connect a small MOSFET, the SENSEFET, in parallel with the Power MOSFET (almost in parallel the drain voltage is enforced by a unity voltage follower.) The SENSEFET now carries a current proportional to that of the Power MOSFET but N times smaller where N is the ratio of the widths of the power MOSFET ot the SENSEFET. A SENSEFET connection is shown in Figure 2.25a. Ratios are usually in the few thousands. In [58] the authors propose

a technique that allows them to exercise a division ratio of over two millions. RDS sensng depends on measurin the voltage drop across the ON resistance of the switch. RDS however is poorly defined and varies nonlinearly with sevral parameters. This method produces an error of 50 – 100%. A schematic is shown in Figure 2.25b [57].

2.8 MOSFET Switch Driving

2.8.1 Tapered Inverter Chain

Tapered inverter chains are usually used to drive high capacitive loads or Input / Output Pads. The Power Stage MOSFETs in Buck converters are a high capacitive load and will be very slow if driven directly by small core logic gates. Optimization for power or delay can be achieved by using a tapered inverter chain [45]. Figure 2.26 shows an adaptive FET scheme combined with a tapered inverter chain. Each inverter is sized by multiplying the previous stages width by a factor m known as the taper factor. Hence the inverters increase exponentially in size. The number and sizes of the inverters and sizes of Power MOSFETs can all be optimized together for minimum delay, minimum power or minimum area overhead or a compromise between the two as shown in [45, 47].

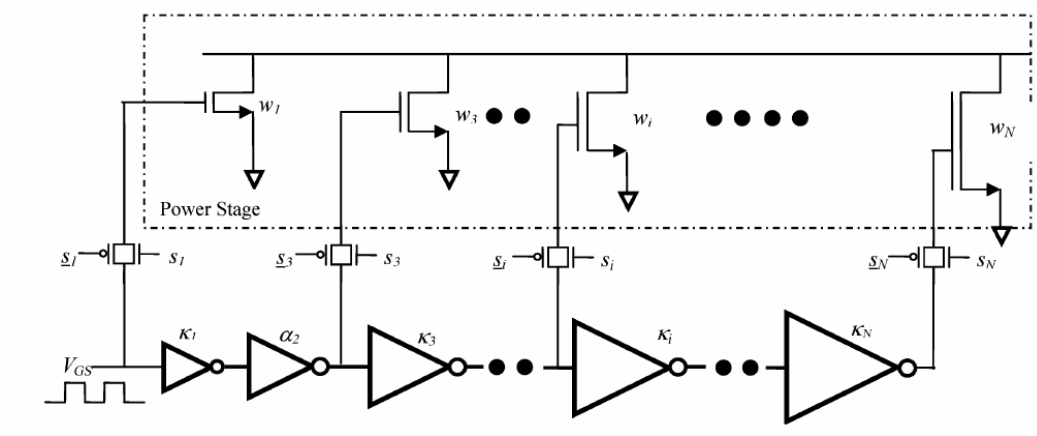


Figure 2.26: Tapered Inverter Chain mixed with and Adaptive FET Sizing Scheme [45]

2.9 Design Considerations

2.9.1 Soft Starting

Since the output capacitor is empty at the beginning an inrush current occurs to charge up this capacitor through the High Side switches. To avoid such a large current a soft start circuit is needed. For PWM controlled circuits gradual ramping of the frequency of operation can server as soft starting. In biomedical applications this is particularly important since the power source itself is limited. In [45] the authors propose a scheme for soft starting based on gradual ramping.

2.9.2 Input Decoupling Capacitor

An input decoupling capacitor is needed to reduce the effect of the current spikes during switching events. Simply stated the decoupling current supplies the surge currents. At high switching frequencies resonance between the input capacitor the input bondwire inductance can occur increasing the effect of the ripple. In such a case the decoupling capacitor needs to be larger or a topology such as the flying capacitor topology that reduces input ripple should be used.

2.9.3 Control Circuitry Supply Generation

The control circuits controlling the power stage, and the sensors and drivers need supply. Common techniques to do this are either: using an external supply (common in academic research since it simplifies a lot of issues), using an LDO for internal voltage rails needed [6], using a switched capacitor circuit to generate the supply [5]. Another option is using the output of the circuit itself. In such a case a startup circuit is needed.

2.9.4 Dead Time

Consider a simple buck converter. Ideally at most one switch is ON. However due to high switching frequencies some instants might occur in which both switches are

ON. In such a case a shoot though current occurs (also known as cross conduction). This causes low of power and large current flow. To avoid this dead time is added. In dead time the inductor can form a current through the NMOS transistor body diode. This also produces a loss. This loss must be minimized by reducing the dead-time. However making the dead time too small increases the possibility of shoot through. In the literature there are several techniques for adjusting dead time: fixed dead time, adaptive dead-time schemes are amongst the most common.

CHAPTER 3

SYSTEM LEVEL MODELLING AND OPTIMIZATION

DC-DC CONVERTERS[1] are widely used in modern electronics and power systems. Converter circuits elements through which power flows from the input(s) to the output(s) are known as the power stage. Modeling the power stage accurately is important in determining the performance metrics of the converter such as: efficiency, output ripple, output voltage regulation and transient response. One of the most common modeling techniques is the state space representation (SS).

Optimizing the converter for efficiency requires carefully and accurately accounting for losses and minimizing them, The major loss components to account for are: conduction losses, switching losses and controller circuit losses. Switching losses are typically straight forward to calculate given switch gate capacitances. Controller circuit losses are typically modeled by a lumped fixed value. Accounting for conduction losses requires precise modeling of the power stage including parasitics such as: power switches ON state resistances, equivalent series resistance (ESR) of capacitors, DC resistance (DCR) of inductors bottom plate parasitics (BPP) of flying capacitors and any other parasitic (inductors or capacitors).

The SS representation can provide: (a) simplified lumped steady-state equivalent circuit model for calculation of losses and propagation [9,59], (b) Sampled Data Model (SDM) for controller design [60] (c) small signal averaged models for stability analysis

[1]This chapter is largely the material of a paper to be submitted to IEEE Transactions on Power Electronics

and compensator design [9] and (d) Discrete-time model for designing digital controllers [36]. The difficulty of obtaining the SS model depends on the complexity of the circuit. For relatively simple converters circuits and relatively simple models of parasitics, the SS equations can be obtained by hand analysis. As the complexity of the circuit increases and/or the complexity of the modeled parasitics, hand derivation becomes increasingly tedious and error-prone.

Prior works attempting to automate the SS derivation include: [36,38,59,61]. Both targeted switched capacitor converters (SCC). The method in [36, 38] requires manually choosing a tree and co-tree from the circuit graph which is error-prone. In [59,61] an automated method is proposed for modeling SCC. Theoretical and experimental results for the equivalent output resistance in [59] are in good agreement except for a peak due to lack of modeling of parasitic inductances. The methods in [36, 38, 59, 61] by design target SCC and do not account for inductors or parasitic inductances.

The complexity of SCC converters comes from the relatively large numbers of components used. In contrast inductive converters (INDC), were relatively simple while achieving high efficiencies (>90%). However, the push for integration, and hence the usage of low quality inductors drives the use of more complex power stage topologies. In [15] two 2nH integrated inductors (with mutual coupling to increase effective inductance) were used in a stacked interleaved buck converter topology. In [12,17] parasitic bondwire inductors are used in a four phase interleaved buck converter. In [2, 62–64] hybrids of INDC/SCC are proposed to reduce the inductor size needed. In [65] a parallel combination of INDC and SCC is used to provide a wider loading range. Accurately modeling the increasingly complex topologies and associated parasitics requires more automation.

In this chapter we present the derivation and implementation of an algorithm for the automated modeling and performance evaluation of switched mode DC-DC converter power stage with controlled switching. The proposed method is able to model complex converters with arbitrary configurations of linear elements such as resistors, capacitors, inductors, mutual inductors and parasitic effects that are represented by arbitrary combinations of linear circuit elements. The proposed algorithm consists

of two sub-algorithms: (i) an automated state space model generator and (ii) an automated performance evaluator. The rest of this paper is organized as follows: the automated state space model generator is discussed in Section 3.1 and Section 3.2, Section 3.3 presents the automated performance evaluators, Section V provides some examples of applying the algorithm,. Section VI discusses some of the limitations of the algorithm and Section VII concludes this paper.

3.1 State Space Matrices Generation: MNA-SS-REDOX Algorithm

The first sub-algorithm concerns the generation of state space matrices. It consists of two parts: MNA-SS-REDOX algorithm, discussed in this section, and the state variables transformation matrices algorithm discussed in the next section.

The MNA-SS-REDOX procedure consists of three stages: preparation stage (Section 3.1.2), modified nodal analysis (MNA) formulation stage (Section 3.1.3) and MNA to SS reduction stage (Section 3.1.4). We collect together a few techniques from the literature to obtain an algorithm or method for automated generation of state space representation. The authors search through the literature has found no one collected description of the algorithm as is presented here. The separate sub-algorithms can be found however in several references. The MNA algorithm can be found in [66]. The algorithm for reduction from MNA to SS form can be found in [67]. In the next sub-section we will revise some state space modeling preliminaries.

3.1.1 State Space Modeling

Modeling refers to putting into mathematical form the relation between variables of interest in a system. One of the most common methods of modeling is the state space representation. The state space representation is based on the idea that any dynamical system's past can be summarized at one point in time by a number of variable. These variables are called state variables. Given these state variables at one instant, one

can predict the future trajectory of that system. Let the state variables be collected together in a vector $\mathbf{x}$ and the inputs of the system be $\mathbf{u}$ and the output be $\mathbf{y}$. Then the state space representation is:

$$\begin{aligned} \dot{\mathbf{x}}(t) &= \mathbf{f}(\mathbf{x}(t), \mathbf{u}(t), t) \\ \dot{\mathbf{y}}(t) &= \mathbf{g}(\mathbf{x}(t), \mathbf{u}(t), t) \end{aligned} \tag{3.1}$$

We will drop the t argument and assume it implicitly except when needed. If the system is known to be Linear Time Invariant (LTI), then we can reduce 3.1 to equations (3.2) and (3.3) where $\mathbf{A}, \mathbf{B}, \mathbf{C}$ and $\mathbf{D}$ are constant matrices [68].

$$\dot{\mathbf{x}} = \mathbf{A}\mathbf{x} + \mathbf{B}\mathbf{u} \tag{3.2}$$

$$\mathbf{y} = \mathbf{C}\mathbf{x} + \mathbf{D}\mathbf{u} \tag{3.3}$$

Power converters are highly nonlinear systems, in particular switched nonlinear systems. However, under the following two assumptions:

1. Controlled Switching: we assume that all switches are driven by signals external to the power stage. Further we assume this switching signal is strong enough that the switch is either ON or OFF.

2. Linear Elements: the passives (inductors and capacitors) are linear and that any associated parasitics are modeled as linear elements.

power converters can be considered LTI systems in each individual phase. Thus each phase can be represented by an equation similar to equations (3.2) and (3.3). The solutions from each phase can be "stitched" together by applying boundary conditions to each phase. The boundary condition simply states that the final state of one phase is the initial condition is the next.

To derive the boundary conditions one has to recall that energy storage elements in the system (capacitors and inductors) resist sudden changes in their state. They require continuity of their state variables (voltage of capacitors and current of inductors). Assume the period of the converter is $[0 - T]$ and there are N phases. Let

$t_0, t_1, t_2, \ldots, t_i, \ldots, t_{N_{PH}}$ be the switching instants of each phase, $t_{N_{PH}} - t_0 = T$, where T is the duration of a complete switching cycle. Assume the state variables of energy storage elements (capacitors and inductors) are collected in a vector $\mathbf{x_c}$ which we will call the *canonical variables vector*. The boundary conditions can be expressed as:

$$\begin{aligned} \mathbf{x_c}(t_1^-) &= \mathbf{x_c}(t_1^+) \\ \mathbf{x_c}(t_2^-) &= \mathbf{x_c}(t_2^+) \\ &\vdots \\ \mathbf{x_c}(t_{N_{PH}}^-) &= \mathbf{x_c}(t_{N_{PH}}^+) \end{aligned} \tag{3.4}$$

Note that the last equation applies between the current period and the next period. The solution of the state space equation equation (3.2) is given by [68]:

$$\mathbf{x}(t) = e^{\mathbf{A}t}\mathbf{x}(0) + \int_0^t e^{\mathbf{A}(t-\tau)}\mathbf{B}\mathbf{u}(\tau)d\tau \tag{3.5}$$

If the input $\mathbf{u}$ can be assumed constant [2] then equation (3.5) can be rewritten as:

$$\mathbf{x}(t) = \mathbf{\Phi}(t)\mathbf{x}(0) + \mathbf{\Gamma}(t)\mathbf{u} \tag{3.6}$$

Where:

$$\begin{aligned} \mathbf{\Phi}(t) &= e^{\mathbf{A}t} \\ \mathbf{\Gamma}(t) &= \int_0^t e^{\mathbf{A}(t-\tau)}\mathbf{B}d\tau = \int_0^t e^{\mathbf{A}(\tau)}\mathbf{B}d\tau \\ &= \mathbf{A}^{-1}(e^{\mathbf{A}t} - \mathbf{I})\mathbf{B} \end{aligned} \tag{3.7}$$

The last simplification assumes $\mathbf{A}$ is invertible. for power converters this is not always the case [59,61]. When $\mathbf{A}$ is not invertible we have to directly carry out the integration.

Note that equation (3.6) can be discretized by taking $t = nT$. This is known as the sampled data model [60, 69]

[2] For integrated converters, to utilize this assumption the converter must use good decoupling capacitors, use low frequencies or the models of the connecting bonding included in the simulated netlist

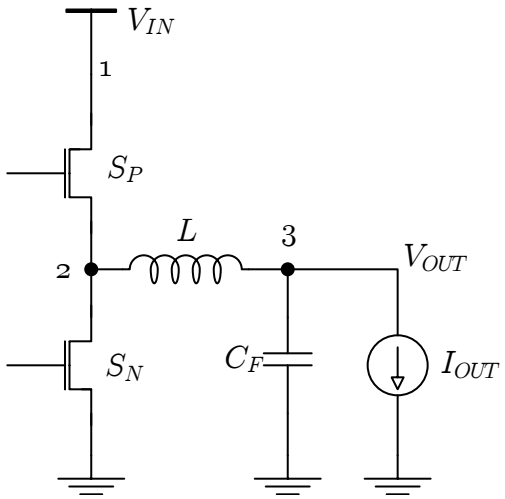


Figure 3.1: Simple Buck Converter Circuit

3.1.2 Preparation Stage

The state space matrices generation sub-algorithm starts with the following inputs: a Netlist $\mathcal{N}$, a switching sequence array $\mathbf{S_{SEQ}}$, a duty ratio array **Duty** and finally T the switching period of the converter. Note that $\mathbf{S_{SEQ}}$ is an $N_{PH} \times N_{SW}$ matrix with elements being 1 for ON and 0 for OFF. N_{PH} is the number of phases of the circuit and N_{SW} is the number of switches in the circuit.

Consider the simple buck converter circuit shown in figure 3.1 operating a frequency of 200KHz and a high side duty ratio of 0.4. The input voltage is 10V, output current of 0.5A, ON state resistance of both switches is 0.1Ω, the $L = 1\mu$H and $C_F = 10\mu$F. The inputs to the algorithm are as follows:

$$\mathcal{N} = \begin{bmatrix} V_{in} & 1 & 0 & 10 \\ I_{out} & 3 & 0 & 0.5 \\ S_P & 1 & 2 & 0.1 \\ S_N & 2 & 0 & 0.1 \\ L & 2 & 3 & 10^{-6} \\ C_F & 3 & 0 & 10^{-5} \end{bmatrix} \qquad \mathbf{S_{SEQ}} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

$$\mathbf{Duty} = \begin{bmatrix} 0.4 & 0.6 \end{bmatrix} \tag{3.8}$$

$$T = 5\mu s$$

The netlist is read like a typical SPICE netlist with the second and third column

indicating the positive and negative nodes of each element respectively.

The preparation stage consists of two sub-steps: OFF switch removal step and dead branch elimination step. In the OFF switch removal step the all switches that are set as off are removed. In the dead branch elimination we remove all branches not reachable from the output or input side of the converter. This is performed by iterating over branches and performing a breadth-first search [70] towards the input source and load. Any branch with no connection is removed from the netlist. Finally if the source itself is disconnected it is removed from the netlist.

All the removed elements form the dead netlist $\mathbf{N_{dead}}$ and the remaining elements form the active netlist $\mathbf{N_{act}}$ The netlist is now ready for MNA analysis.

3.1.3 Modified Nodal Analysis Stage

MNA is a de facto standard method of analysis because of its use in SPICE. It is used because of its relative simplicity. Although proofs and derivations on the method require some graph theory, implementation of the method requires no graphs at all. Thus it is relatively easy to implement. We present here a simplified sketch of the derivation that allows us to implement the method. The derivation here is adapted from [66].

Let a circuit be composed of b branches and connected at n nodes. Mark all branches by a nominal current direction. The incidence matrix $\mathbf{A_{inc}}$ is an $(n-1) \times b$ matrix formed according to the following rule. Consider a node i and a branch j then the element a_{ij} is given by:

$$\mathbf{A_{inc}} := a_{ij} = \begin{cases} +1 & \text{branch } j \text{ current leaves node } i \\ -1 & \text{branch } j \text{ current enters node } i \\ 0 & \text{branch } j \text{ not connected to node } i \end{cases} \tag{3.9}$$

If $\mathbf{I}$ is defined as a vector of all branch currents:

$$\mathbf{I} = [I_1, I_2, \ldots, I_b]\,. \tag{3.10}$$

Then Kirchoff's current law can be expressed as:

$$\mathbf{A_{inc}I} = \mathbf{0} \tag{3.11}$$

Each column of the incidence matrix represents a single branch element. For branch j connected to nodes n_1 and n_2 respectively there will be a $+1$ at row n_1 and -1 at row n_2. In general, for a two terminal element there will be at most one $+1$ entry and one -1 entry per column. The branch voltage is given by:

$$V_{bj} = V_{n1} - V_{n2} \tag{3.12}$$

We can generalize this to relate all branch voltages $\mathbf{V_b}$ to node voltages $\mathbf{V_n}$ by:

$$\mathbf{V_b} = \mathbf{A_{inc}^t V_n} \tag{3.13}$$

Two terminal circuit elements can be grouped into three categories:

1. Group-I elements (G1) which have an admittance description that requires no integration of branch voltages, for example capacitors and resistors.

2. Group-II elements (G2) elements not in G1 and not current sources (inductors, mutual inductors and voltage sources).

3. Group-III elements (G3) current sources.

The incidence matrix and branch currents vector can partitioned into three parts, one for each group.

$$\mathbf{A_{inc}I} = \begin{bmatrix} \mathbf{A_1} & \mathbf{A_2} & \mathbf{A_3} \end{bmatrix} \begin{bmatrix} \mathbf{I_1} \\ \mathbf{I_2} \\ \mathbf{I_3} \end{bmatrix} = 0 \tag{3.14}$$

Similarly the voltages relation can be partitioned into:

$$\begin{bmatrix} \mathbf{V_1} \\ \mathbf{V_2} \\ \mathbf{V_3} \end{bmatrix} = \begin{bmatrix} \mathbf{A_1^t} \\ \mathbf{A_2^t} \\ \mathbf{A_3^t} \end{bmatrix} \mathbf{V_n} \tag{3.15}$$

The constitutive equations of elements in each group are:

$$\text{G1:} \quad \mathbf{Y_1 V_1} = \mathbf{I_1} \tag{3.16}$$

$$\text{G2:} \quad \mathbf{Y_2 V_2 + Z_2 I_2} = \mathbf{W_2} \tag{3.17}$$

$$\text{G3:} \quad \mathbf{I_3} = \mathbf{J} \tag{3.18}$$

Where $\mathbf{W_2}$ is the vector of voltage sources and $\mathbf{J}$ is the vector of current sources. Rewriting equation (3.14) as:

$$\mathbf{A_1 I_1 + A_2 I_2 = -A_3 J} \tag{3.19}$$

Substituting from (3.15), (3.16) into (3.19) and from (3.15) into (3.17) we get:

$$\mathbf{A_1 Y_1 A_1^t V_n + A_2 I_2 = -A_3 J} \tag{3.20}$$

$$\mathbf{Y_2 A_2^t V_n + Z_2 I_2 = W_2} \tag{3.21}$$

$$\begin{bmatrix} \mathbf{A_1 Y_1 A_1^t} & \mathbf{A_2} \\ \mathbf{Y_2 A_2^t} & \mathbf{Z_2} \end{bmatrix} \begin{bmatrix} \mathbf{V_n} \\ \mathbf{I_2} \end{bmatrix} = \begin{bmatrix} \mathbf{-A_3 J} \\ \mathbf{W_2} \end{bmatrix} \tag{3.22}$$

In a more condensed form as:

$$\mathbf{T X_{MNA} = U} \tag{3.23}$$

Equation (3.23) is the final form of MNA equation.

Note that $\mathbf{Y_1}$ and $\mathbf{Z_2}$ contain terms of the form $C_i D$ and $L_j D$ where D is the differential operator d/dt. These terms come from capacitors and inductors.

3.1.4 MNA to SS Reduction

We now want to transform the MNA system into state space equations. The equations are of the form:

$$\begin{aligned} \mathbf{X_S} &= \mathbf{A}\mathbf{X_S} + \mathbf{B}\mathbf{S} \\ \mathbf{Y_S} &= \mathbf{C}\mathbf{X_S} + \mathbf{D}\mathbf{S} \end{aligned} \tag{3.24}$$

Where $\mathbf{X_S}$ are the state space variables, $\mathbf{Y_S}$ are the desired outputs (unknown voltages or currents) and $\mathbf{S}$. $\mathbf{S}$ is the sources vector and depends on how the load is represented. We will continue this derivation with the assumption of a single input single output converter, where the load is represented by a current source similar to the figure 3.1. In this case

$$\mathbf{S} = \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix} \tag{3.25}$$

Other loads voltage source loads can be accomodated with slight modifications. [3]

The algorithm we will use to accomplish this conversion is from [67]. The proof provided here is slightly modified to be slightly more general and make the treatment of the singular matrices more clear. Due to the way we partitioned the elements into groups (G1 — G3) we know that T contains only constants or derivative operator pre-multiplied by constants. In fact we can seperate T as follows:

$$\mathbf{T} = G + \mathbf{Q}D \tag{3.26}$$

$\mathbf{Q}$ contains coefficients of derivative terms and the rest (constants) are in $\mathbf{G}$. Further $\mathbf{U}$ can be split into a sources term $\mathbf{S}$ and a premultiplier $\mathbf{S}$.

$$\mathbf{U} = \mathbf{K}\mathbf{S} \tag{3.27}$$

The MNA equation equation (3.23) can now be rewritten as:

$$(\mathbf{G} + \mathbf{Q}D)\mathbf{X_{MNA}} = \mathbf{K}\mathbf{S} \tag{3.28}$$

[3] Passive element loads will already absorbed in the $\mathbf{A}$ and $\mathbf{B}$ matrices.

In anticipation of the recursive nature of this algorithm we will rewrite equation (3.28) as:

$$(\mathbf{G^0} + \mathbf{Q^0}D)\mathbf{X^0} = \mathbf{K^0S} \tag{3.29}$$

Instead of tackling this form directly we will rewrite it as:

$$(\mathbf{G^n} + \mathbf{Q^n}D)\mathbf{X^n} = \sum_{m=0}^{r} \mathbf{K_m^n} D^m \mathbf{S} \tag{3.30}$$

Where D is again the differential operator. Note that equation (3.28) is a special case of equation (3.30) with $r = 0$ and $n = 0$. The steps now to obtain the SS form are as follows:

1. If $\mathbf{Q^n}$ is non-singular then we can immediately obtain:

   (1) SS variables:

   $$\mathbf{X_S} = \mathbf{X^n} \tag{3.31}$$

   (2) SS coefficients as:

   $$\begin{aligned} \mathbf{A} &= -(\mathbf{Q^n})^{-1}\mathbf{G^n} \\ \mathbf{B} &= (\mathbf{Q^n})^{-1}\mathbf{K_0^n} \end{aligned} \tag{3.32}$$

   (3) In addition there are source derivative coefficients given by[4]:

   $$\mathbf{B_{dm}} = (\mathbf{Q^n})^{-1}\mathbf{K_m^n}, \quad \text{for} \quad m = 1, 2, ..., r+1 \tag{3.33}$$

   We then skip Steps (2) and (3). If $\mathbf{Q^n}$ is singular then we proceed to Step (2).

2. We now perform elementary row operations on $\mathbf{Q^n}$ to reduce it to reduced row echelon form (RREF). The same operations are performed on $\mathbf{G^n}$ and $\mathbf{K_m^n}$ such that equality is preserved. Since $\mathbf{Q^n}$ is singular we know that there will be at

[4]The source derivative terms can be ignored if the input source is assumed constant i.e. DC and with very small resistance. The other options is ofcourse to include the source imperfections in the netlist.

least one zero row at the end. $\mathbf{G^n}$, $\mathbf{Q^n}$ and $\mathbf{K_m^n}$ can now be rewritten as:

$$\begin{aligned} \mathbf{Q^n} &= \begin{bmatrix} \mathbf{Q_{11}^n} & \mathbf{Q_{12}^n} \\ 0 & 0 \end{bmatrix} \quad \mathbf{G^n} = \begin{bmatrix} \mathbf{G_{11}^n} & \mathbf{G_{12}^n} \\ \mathbf{G_{21}^n} & \mathbf{G_{22}^n} \end{bmatrix} \\ \mathbf{X^n} &= \begin{bmatrix} \mathbf{X_1^n} \\ \mathbf{X_2^n} \end{bmatrix} \qquad\qquad \mathbf{K_m^n} = \begin{bmatrix} \mathbf{K_{m1}^n} \\ \mathbf{K_{m2}^n} \end{bmatrix} \end{aligned} \tag{3.34}$$

If $\mathbf{G_{22}^n}$ is non-singular proceed to Step (3). If $\mathbf{G_{22}^n}$ is singular then:

(1) Reduce the composite matrix $\begin{bmatrix} \mathbf{G_{21}^n} & \mathbf{G_{22}^n} \end{bmatrix}$ into row echelon form while applying similar operations to $\mathbf{K_{m2}^n}$

(2) Since $\begin{bmatrix} \mathbf{G_{21}^n} & \mathbf{G_{22}^n} \end{bmatrix}$ is in RREF form we know that there will be columns of the identity matrix. Swap these into the location of $\mathbf{G_{22}^n}$. To keep the equation valid the same columns in $\mathbf{G_{11}^n}, \mathbf{G_{12}^n}, \mathbf{Q_{11}^n}, \mathbf{Q_{12}^n}$ must be swapped.

(3) Further the elements in $\mathbf{X_1^n}, \mathbf{X_2^n}$ corresponding to the swapped columns are also swapped. At this point we generate the matrix $\mathbf{P^n}$ which reverses the element swappings of $\mathbf{X_1^n}, \mathbf{X_2^n}$. The matrix $\mathbf{P^n}$ can be obtained by applying the swappings to a suitably sized identity matrix.

3. We now calculate the matrices $\mathbf{G^{n+1}}, \mathbf{Q^{n+1}}, \mathbf{K_m^{n+1}}$ and $\mathbf{X^{n+1}}$ for the equation:

$$(\mathbf{G^{n+1}} + \mathbf{Q^{n+1}}D)\mathbf{X} = \sum_{m=0}^{r+1} \mathbf{K_m^{n+1}} D^m \mathbf{S} \tag{3.35}$$

using the following formulae:

$$\begin{aligned} \mathbf{X^{n+1}} &= \mathbf{X_1^n} \\ \mathbf{G^{n+1}} &= \mathbf{G_{11}^n} - \mathbf{G_{12}^n}(\mathbf{G_{22}^n})^{-1}\mathbf{G_{21}^n} \\ \mathbf{Q^{n+1}} &= \mathbf{Q_{11}^n} - \mathbf{Q_{12}^n}(\mathbf{G_{22}^n})^{-1}\mathbf{G_{21}^n} \end{aligned} \tag{3.36}$$

and

$$\mathbf{K_m^{n+1}} = \begin{cases} \mathbf{K_{m1}^n} - \mathbf{G_{12}^n}(\mathbf{G_{22}^n})^{-1}\mathbf{K_{m2}^n} & m = 0 \\ \mathbf{K_{m1}^n} - \mathbf{G_{12}^n}(\mathbf{G_{22}^n})^{-1}\mathbf{K_{m2}^n} & \\ \quad -\mathbf{Q_{12}^n}(\mathbf{G_{22}^n})^{-1}\mathbf{K_{(m-1)2}^n} & m = 1 \ldots r \\ -\mathbf{Q_{12}^n}(\mathbf{G_{22}^n})^{-1}\mathbf{K_{(m-1)2}^n} & m = r+1 \end{cases} \tag{3.37}$$

We now go back to Step (1). Note that equation (3.35) is the same as equation (3.30) with n set as $n+1$ and r set as $r+1$.

The formulae in equations (3.36) and (3.37) can be proved by using equation (3.34) in equation (3.30). This gives:

$$\begin{aligned} \left(\begin{bmatrix} \mathbf{G_{11}^n} & \mathbf{G_{12}^n} \\ \mathbf{G_{21}^n} & \mathbf{G_{22}^n} \end{bmatrix} + \begin{bmatrix} \mathbf{Q_{11}^n} & \mathbf{Q_{12}^n} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \frac{d}{dt} \right) \begin{bmatrix} \mathbf{X_1^n} \\ \mathbf{X_2^n} \end{bmatrix} \\ = \sum_{m=0}^{r} \begin{bmatrix} \mathbf{K_{m1}^n} \\ \mathbf{K_{m2}^n} \end{bmatrix} D^m \mathbf{S} \end{aligned} \tag{3.38}$$

Writing out the lower row and solving for $\mathbf{X_2^n}$ we have:

$$\mathbf{X_2^n} = (\mathbf{G_{22}^n})^{-1} \left(\sum_{m=0}^{r} \begin{bmatrix} \mathbf{K_{m1}^n} \\ \mathbf{K_{m2}^n} \end{bmatrix} D^m \mathbf{S} - \mathbf{G_{21}^n} \mathbf{X_1^n} \right) \tag{3.39}$$

Writing out the upper row of equation (3.38) and substituting equation (3.39) we get (after some algebra) equation (3.35) with the coefficients given by equations (3.36) and (3.37). We are now able to obtain the SS equations for a circuit in any of its phases. The coefficients of the output equation $\mathbf{C}$ and $\mathbf{D}$ are selected based upon the

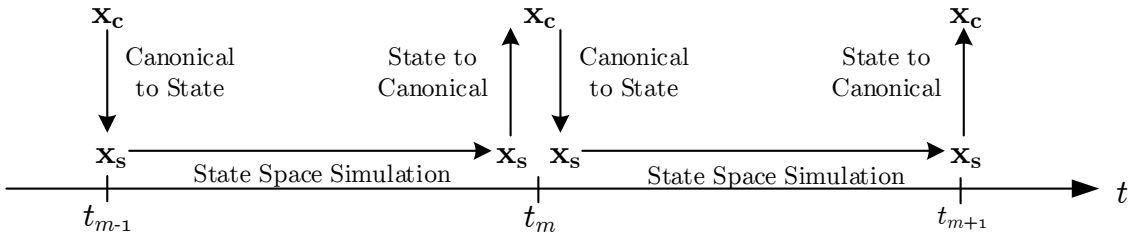


Figure 3.2: Moving from phase to phase requires converting to canonical state variables then to the next phases state variables

variables (voltages and currents) needed.

3.2 State Space Matrices Generation: State Variables Transformation Matrices

The algorithm presented in the previous Section shows how to get the state space equations for each phase. However the state variables chosen by the algorithm will not be the same in every phase. Hence the boundary conditions (BC) equation (3.4) cannot be directly applied. To be able to apply these BCs we must select a vector of circuit variables that is continuous. The easiest set to pick are the canonical variables $\mathbf{x_c}$.

Assume we are analyzing phase m which extends from $[t_{m-1} - t_m]$. Assume we have the values of the canonical state variables at time t_{m-1}, i.e. $\mathbf{x_c}(t_{m-1})$. From these we can compute phase m state variables at that same point in time $\mathbf{X_s}(t_{m-1})$. Now we can simulate the phase using equations equation (3.24). We can calculate up to the last time point in the phase i.e. t_m. Then we convert these state variables $\mathbf{X_s}(t_m)$ back to canonical variables $\mathbf{x_c}(t_m)$. The process is then repeated for the next phase. This process is shown in figure 3.2. The mathematical details for converting from canonical to state variables and vice versa are presented next.

Since phase m spans $[t_{m-1} - t_m]$, the canonical and state variables at these time points are $\mathbf{x_c}(t_{m-1})$, $\mathbf{x_c}(t_m)$, $\mathbf{X_s}(t_{m-1})$ and $\mathbf{X_s}(t_m)$. Initially, $\mathbf{x_c}(t_{m-1})$ is known. Conversion will require us to pass through the MNA equation system. We will denote

the MNA unknowns vector as $\mathbf{X_{MNA}}(t)$ which is composed of node voltages and G2 currents. Also we assume that $\mathbf{x_c(t)}$ is sorted such that capacitor voltages are at the top followed by inductor currents. Where $\mathbf{v_c}(t)$ are all the capacitor voltages, $\mathbf{i_L}(t)$ are all the inductor currents, $\mathbf{V_n}(t)$ are the active nodal voltages (i.e. not belonging to the dead part of the circuit) and $\mathbf{v_{c,act}}(t)$, $\mathbf{i_{L,act}}(t)$ are the active capacitor voltages and inductor currents respectively. We will also need to refer to active canonical variables $\mathbf{x_{c,act}}$ which are canonical variables for elements in the active netlist $\mathbf{N_{act}}$.

$$\begin{aligned} \mathbf{x_{MNA}}(t) = \begin{bmatrix} \mathbf{V_n}(t) \\ \mathbf{i_2}(t) \end{bmatrix} = \begin{bmatrix} \mathbf{V_n}(t) \\ \mathbf{i_{L,act}}(t) \\ \mathbf{i_{V_{in}}}(t) \end{bmatrix} \\ \mathbf{x_c}(t) = \begin{bmatrix} \mathbf{v_c}(t) \\ \mathbf{i_L}(t) \end{bmatrix}, \quad \mathbf{x_{c,act}}(t) = \begin{bmatrix} \mathbf{v_{c,act}}(t) \\ \mathbf{i_{L,act}}(t) \end{bmatrix} \end{aligned} \tag{3.40}$$

Frequently during the derivation we will refer to an *appropriate selection matrix*. A selection matrix is a matrix composed of only zeros and ones. The ones are placed such that we take only the elements we need and discard the rest. For example to extract only the active canonical elements from the complete canonical vector we can use a matrix $\mathbf{F_{act}}$ such that:

$$\mathbf{x_{c,act}} = \mathbf{F_{act}}\mathbf{x_c} \tag{3.41}$$

3.2.1 Canonical to State Variables Transformation

To obtain the state variables at point t_{m-1} we need to recognize that:

- All elements of $\mathbf{X_S}$ are also elements of $\mathbf{X_{MNA}}$ hence they are either node voltages, inductor currents or voltage source currents. Since $\mathbf{x_c}$ contains inductor currents, they can be obtained immediately.

$$\mathbf{X_{S,L}} = \mathbf{F_{L,act}}\mathbf{x_c} \tag{3.42}$$

  Where $\mathbf{X_{S,L}}$ is the state vector $\mathbf{X_S}$ with variables other than inductor currents

set to zero and $\mathbf{F_{L,act}}$ is an appropriate selection matrix.

- To obtain the node voltages and voltage source currents we observe that capacitors and inductors will resist changes in their state. Thus for all purposes at the switching instant i.e., time change from t_{m-1}^{-} to t_{m-1}^{+}, at start of phase m the capacitors can be considered as voltages sources and inductors as current sources.

Replacing capacitors with voltages sources and inductors with current sources we can solve the circuit at that instant (t_{m-1}) and obtain nodal voltages and voltage source currents we need. Since all variables are the same time instant we will drop the t_{m-1} argument.

This can be mathematically stated as follows: in the active Netlist $\mathbf{N_{act}}$ replace all capacitors with voltages sources and inductors with current sources to obtain a new netlist $\mathbf{N_{IC}}$ (inital conditions netlist). We then perform MNA analysis on this netlist. We get an MNA equation similar to equation (3.22) with a few exceptions: $\mathbf{Z_2} = \mathbf{0}$ since there are no inductors (they are current sources now) and $\mathbf{Y_2}$ is an identity matrix $\mathbf{I}$. Thus the equations can be written as:

$$\begin{bmatrix} \mathbf{A_1 Y_1 A_1^t} & \mathbf{A_2} \\ \mathbf{A_2^t} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{V_n} \\ \mathbf{I_2} \end{bmatrix} = \begin{bmatrix} \mathbf{-A_3 J} \\ \mathbf{W_2} \end{bmatrix} \tag{3.43}$$

We can split the G2 elements (voltages sources) into two groups: voltage source that where originally capacitors and the input source. The G2 matrices look as follows:

$$\begin{aligned} \mathbf{A_2} &= \begin{bmatrix} \mathbf{A_{2C}} & \mathbf{A_{2}}_{V_{in}} \end{bmatrix} \\ \mathbf{W_2} &= \begin{bmatrix} \mathbf{W_{2C}} \\ \mathbf{W_{2}}_{V_{in}} \end{bmatrix} = \begin{bmatrix} \mathbf{v_{c,act}} \\ V_{in} \end{bmatrix} \\ \mathbf{I_2} &= \begin{bmatrix} \mathbf{I_{2C}} \\ I_{V_{in}} \end{bmatrix} \end{aligned} \tag{3.44}$$

We can also similarly split G3 elements into the original load current source I_{out} and the current sources that are actually inductors. Therefore:

$$\begin{aligned} \mathbf{A_3} &= \begin{bmatrix} \mathbf{A_{3L}} & \mathbf{A}_{\mathbf{3}I_{out}} \end{bmatrix} \\ \mathbf{J} &= \begin{bmatrix} \mathbf{I_{L,act}} \\ I_{out} \end{bmatrix} \end{aligned} \tag{3.45}$$

Substituting equations (3.44) and (3.45) into equation (3.43) we have for the RHS:

$$\begin{aligned} \begin{bmatrix} -\mathbf{A_3 J} \\ \mathbf{W_2} \end{bmatrix} &= \begin{bmatrix} -\mathbf{A_{3L}} \mathbf{I_{L,act}} \\ \mathbf{v_{c,act}} \\ 0 \end{bmatrix} + \begin{bmatrix} -\mathbf{A_{3J}} I_{out} \\ 0 \\ V_{in} \end{bmatrix} \\ &= \begin{bmatrix} \mathbf{0} & -\mathbf{A_{3L}} \\ \mathbf{I} & \mathbf{0} \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{v_{c,act}} \\ \mathbf{i_{L,act}} \end{bmatrix} + \begin{bmatrix} 0 & -\mathbf{A_{3J}} \\ 0 & 0 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix} \\ &= \mathbf{F_c x_{c,act}} + \mathbf{F_S S} \\ &= \mathbf{F_c F_{act} x_c} + \mathbf{F_S S} \end{aligned} \tag{3.46}$$

and for the LHS:

$$\begin{aligned} &= \begin{bmatrix} \mathbf{A_1 Y_1 A_1^t} & \mathbf{A_2} \\ \mathbf{A_2^t} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{V_n} \\ \mathbf{I_2} \end{bmatrix} \\ &= \begin{bmatrix} \mathbf{A_1 Y_1 A_1^t} & \mathbf{A_{2C}} & \mathbf{A}_{\mathbf{2}V_{in}} \\ \mathbf{A_{2C}^t} & \mathbf{0} & \mathbf{0} \\ \mathbf{A}_{\mathbf{2}V_{in}}^{\mathbf{t}} & \mathbf{0} & 0 \end{bmatrix} \begin{bmatrix} \mathbf{V_n} \\ \mathbf{I_{2C}} \\ I_{V_{in}} \end{bmatrix} \\ &= \mathbf{T_{IC}} \mathbf{X_{MNA,IC}} \end{aligned} \tag{3.47}$$

We have named the unknowns vector resulting from this modified netlist, $\mathbf{N_{IC}}$, as $\mathbf{X_{MNA,IC}}$ to differentiate it from the unknowns vector of the MNA system extracted from $\mathbf{N_{act}}$. Note however that the needed node voltages and voltages source currents

are contained in $\mathbf{X_{MNA,IC}}$.

We can now express $\mathbf{X_{MNA,IC}}$ as:

$$\mathbf{X_{MNA,IC}} = \mathbf{T_{IC}}^{-1} \left(\mathbf{F_c F_{act} x_c} + \mathbf{F_S S} \right) \tag{3.48}$$

We then use an appropriate selection matrix to extract the desired node voltages and voltage source currents. Call this matrix $\mathbf{F_{nv,vs}}$. Thus:

$$\mathbf{X_{S,nv,vs}} = \mathbf{F_{nv,vs} X_{MNA,IC}} \tag{3.49}$$

Combining equations (3.42) and (3.49) we have:

$$\mathbf{X_S} = \mathbf{F_{nv,vs} X_{MNA,IC}} + \mathbf{F_{L,act} x_c} \tag{3.50}$$

Using equation (3.48) in equation (3.50) gives:

$$\mathbf{X_S} = \mathbf{M x_c} + \mathbf{NS} \tag{3.51}$$

Where:

$$\begin{aligned} \mathbf{M} &= \left(\mathbf{F_{nv,vs}} \mathbf{T_{IC}}^{-1} \mathbf{F_c F_{act}} + \mathbf{F_{L,act}} \right) \\ \mathbf{N} &= \left(\mathbf{F_{nv,vs}} \mathbf{T_{IC}}^{-1} \mathbf{F_S} \right) \end{aligned} \tag{3.52}$$

As can be seen equation (3.51) transforms from the canonical vector and source into the state variables. Note that this equation is linear in $\mathbf{x_c}$ and $\mathbf{S}$.

3.2.2 State To Canonical Variables Transformation

The transformation from state variables to canonical variables is needed at the end of phase m ie.. at point $t = t_m$. We want to obtain $\mathbf{x_c}(t_m)$. We have the values of $\mathbf{X_S}(t_m)$, $\mathbf{x_c}(\mathbf{t_{m-1}})$ and $\mathbf{S}$. Note that the $\mathbf{x_c}$ consists of two parts: the active part and the dead part.

Assume that $\mathbf{x_{c,dead}}$ is the same as $\mathbf{x_c}$ with the active variables zeroed out. Also assume that $\mathbf{x_{c,a}}$ is the same as $\mathbf{x_c}$ with the dead variables zeroed out. Thus $\mathbf{x_c}$ can

be expressed as:

$$\mathbf{x_c} = \mathbf{x_{c,dead}} + \mathbf{x_{c,a}} \tag{3.53}$$

For the dead part we note the following:

- Inductors in the dead part of the circuit have a current of zero (by definition).
- Capacitors in the dead part will have no change in their voltage, i.e. the voltage at t_m is the same as that at t_{m-1}.

Let $\mathbf{Q_{c,dead}}$ be a matrix that selects only dead capacitors from $\mathbf{x_c}$ and leaves the rest. We have:

$$\mathbf{x_{c,dead}}(t_m) = \mathbf{Q_{c,dead}}\mathbf{x_c}(t_{m-1}) \tag{3.54}$$

For the active part we need to convert the state vector $\mathbf{X_S}(t_m)$ into the MNA vector $\mathbf{X_{MNA}}$. This can be accomplished by retracing the MNA to SS Reduction backwards. Assume that the MNA to SS reduction process took n iterations. We then know that $\mathbf{X_S}$ is the same as $\mathbf{X_1^n}$. $\mathbf{X_1^n}$ is related to $\mathbf{X_2^n}$ through equation (3.39). Concatenating $\mathbf{X_1^n}$ and $\mathbf{X_2^n}$ we obtain $\hat{\mathbf{X}}^\mathbf{n}$. Which is the same as $\mathbf{X_1^n}$ except for the possibility of element re-orderings. The reordering can be reversed by the matrix $\mathbf{P^n}$ (see section 3.1.4, item 2c). Thus:

$$\begin{aligned}
\mathbf{X^n} &= \mathbf{P^n}\hat{\mathbf{X}}^\mathbf{n} \\
&= \mathbf{P^n}\begin{bmatrix} \mathbf{X_1^n} \\ \mathbf{X_2^n} \end{bmatrix} \\
&= \mathbf{P^n}\begin{bmatrix} \mathbf{X_1^n} \\ (\mathbf{G_{22}^n})^{-1}\left(\sum_{m=0}^{r}\mathbf{K_m^n}D^m\mathbf{S} - \mathbf{G_{21}^n}\mathbf{X_1^n}\right) \end{bmatrix}
\end{aligned} \tag{3.55}$$

This can be rewritten as[5]:

$$\mathbf{X^n} = \mathbf{R_S^n}\mathbf{S} + \mathbf{R_X^n}\mathbf{X_1^n} \tag{3.56}$$

[5]We are slightly abusing the derivative notation.

Where:

$$\begin{aligned}\mathbf{R_S^n} &= \mathbf{P^n}\begin{bmatrix}\mathbf{0}\\(\mathbf{G_{22}^n})^{-1}\sum_{m=0}^{r}\mathbf{K_m^n}D^m\end{bmatrix}\\ \mathbf{R_X^n} &= \mathbf{P^n}\begin{bmatrix}\mathbf{I}\\-(\mathbf{G_{22}^n})^{-1}\mathbf{G_{21}^n}\end{bmatrix}\end{aligned} \tag{3.57}$$

Since $X^{n-1} = X_1^n = X_S$, with some algebraic manipulation, we have:

$$\mathbf{X^{n-1}} = \left(\mathbf{R_S^{n-1}} + \mathbf{R_X^{n-1}R_S^n}\right)\mathbf{S} + \mathbf{R_X^{n-1}R_X^n X_S} \tag{3.58}$$

Recursively doing this we have:

$$\begin{aligned}\mathbf{X^{n-q}} = &\left[\sum_{j=0}^{q}\left(\prod_{i=1}^{j}\mathbf{R_X}^{n-q+i-1}\right)\mathbf{R_S}^{n-q+j}\right]\mathbf{S}\\ &+\left(\prod_{j=0}^{q-1}\mathbf{R_X}^{n-q+j}\right)\mathbf{X_S}\end{aligned} \tag{3.59}$$

Setting $q = n$ gives and noting that $\mathbf{X^0}$ is $\mathbf{X_{MNA}}$:

$$\mathbf{X_{MNA}} = \mathbf{X^0} = \mathbf{LS} + \mathbf{QX_S} \tag{3.60}$$

Where

$$\begin{aligned}\mathbf{L} &= \left[\sum_{j=0}^{n}\left(\prod_{i=1}^{j}\mathbf{R_X}^{i-1}\right)\mathbf{R_S}^{j}\right]\\ \mathbf{Q} &= \left(\prod_{j=0}^{n-1}\mathbf{R_X}^{j}\right)\end{aligned} \tag{3.61}$$

Recalling that $\mathbf{X_{MNA}}$ is $\begin{bmatrix}\mathbf{V_n} & \mathbf{i_{L,act}} & \mathbf{i_{V_{in}}}\end{bmatrix}^T$ we note that the active inductor currents, $\mathbf{i_{L,act}}$, are immediately available. To get the capacitor voltages, we use only the portion of the incidence matrix that corresponds to the capacitors. We will denote

this portion $\mathbf{A_{1C}}$ such that $\mathbf{v_{c,act}} = \mathbf{A_{1C}V_n}$

$$\begin{aligned}\mathbf{x_{c,act}} &= \begin{bmatrix} \mathbf{A_{1C}} & \mathbf{0} & \mathbf{0} \\ \mathbf{0} & \mathbf{I} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{V_n} \\ \mathbf{i_{L,act}} \\ \mathbf{i_{V_{in}}} \end{bmatrix} \\ &= \mathbf{Q_{1C}X_{MNA}}\end{aligned} \tag{3.62}$$

We finally need to select the active elements into their appropriate positions in $\mathbf{x_{c,a}}$ using an appropriate selection matrix, $\mathbf{Q_{act}}$:

$$\mathbf{x_{c,a}} = \mathbf{Q_{act}x_{c,act}} \tag{3.63}$$

Finally combining the dead and active part:

$$\begin{aligned}\mathbf{x_c}(t_m) &= \mathbf{x_{c,dead}} + \mathbf{x_{c,a}} \\ &= \mathbf{Q_{c,dead}x_c}(t_{m-1}) + \mathbf{Q_{act}Q_{1C}X_{MNA}} \\ &= \mathbf{Q_{c,dead}x_c}(t_{m-1}) + \mathbf{Q_{act}Q_{1C}}\left(\mathbf{LS} + \mathbf{QX_S}\right)\end{aligned} \tag{3.64}$$

Hence:

$$\mathbf{x_c}(t_m) = \mathbf{Q_{c,dead}x_c}(t_{m-1}) + \mathbf{Q_X X_S}(t_m) + \mathbf{Q_S S} \tag{3.65}$$

Where:

$$\begin{aligned}\mathbf{Q_X} &= \mathbf{Q_{act}Q_{1C}Q} \\ \mathbf{Q_S} &= \mathbf{Q_{act}Q_{1C}L}\end{aligned} \tag{3.66}$$

Equation (3.65) transforms the state variables at t_m, the source and canonical variables at t_{m-1} to the canonical variables at t_m.

3.3 Automated Calculation of Steady State Parameters

Generating the state space model is an important step in itself. However further analyses are necessary to properly design the converter power stage. Parameters

such as efficiency, output impedance and regulation are steady state parameters and do not need full time domain (transient) analysis to obtain them. Building on the formulations in sections 3.1 and 3.2 and following similar methods to those in [59,61] we present procedures to obtain steady state performance parameters.

3.3.1 Calculating the Canonical State Vector at Steady State

In this section we will be dealing with more than one phase simultaneously; thus to avoid confusion we will add a superscript to to matrices and vectors ($\mathbf{A^m}$) to identify in which phase they belong. Note that the canonical variables vector $\mathbf{x_c}$ needs no superscript since it is universal for all phases. We start by summarizing the results we have until now:

1. Given the canonical variables at the start of phase $\mathbf{x_c}(t_{m-1})$ and the sources vector $\mathbf{S}$ we can obtain the phase state variables $\mathbf{x_s}(t_{m-1})$, using equation (3.51) which we give the short hand notation:

$$\begin{aligned} \mathbf{X_s^m}(t_{m-1}) &= T_{CS}^m[\mathbf{x_c}(t_{m-1}),\ \mathbf{S}] \\ &= \mathbf{M^m x_c}(t_{m-1}) + \mathbf{N^m S} \end{aligned} \tag{3.67}$$

   T_{CS}: indicates canonical to state transformation.

2. We are able to automatically obtain the state space representation using the method in sections 3.1 and 3.2. The results are matrices $\mathbf{A^m}$ and $\mathbf{B^m}$ for each phase from which $\mathbf{\Phi^m}$ and $\mathbf{\Gamma^m}$. Recall that phase m extends from t_{m-1} to t_m. Given the initial state vector $\mathbf{x_s^m}(t_{m-1})$, the final value of the state vector $\mathbf{x_s^m}(t_m)$ can be obtained using equation (3.6):

$$\begin{aligned} \mathbf{X_s^m}(t_m) = \mathbf{\Phi^m}(t_m - t_{m-1})\mathbf{X_s^m}(t_{m-1}) \\ +\mathbf{\Gamma^m}(t_m - t_{m-1})\mathbf{S} \end{aligned} \tag{3.68}$$

   Note that we replaced input $\mathbf{u}$ with the sources vector $\mathbf{S}$.

3. Given the final state vector of phase m, $\mathbf{x_s^m}(t_m)$, the initial canonical vector for

that phase, $\mathbf{x_c}(t_{m-1})$ and the sources vector $\mathbf{S}$, we can calculate the canonical variables at the end of the phase using equation (3.65) which we give the short hand notation:

$$\begin{aligned}\mathbf{x_c}(t_m) &= T^m_{SC}[\mathbf{x_c}(t_{m-1}),\ \mathbf{X^m_s}(t_m),\ \mathbf{S}] \\ &= \mathbf{Q^m_{c,dead}}\mathbf{x_c}(t_{m-1}) + \mathbf{Q^m_X}\mathbf{X^m_S}(t_m) \\ &\quad + \mathbf{Q^m_S}\mathbf{S}\end{aligned} \tag{3.69}$$

T_{SC}: indicates state to canonical transformation.

Iterating over the phases from $m = 1$ till $m = N_{PH}$, we can chain equations (3.67) to (3.69) (in that order) to move to the next period of the converter. To clarify this assume $N_{PH} = 2$, a total period of T with Phase 1 extending from t_0 to t_1 and Phase 2 from t_1 to t_2. Notice that $T = t_2 - t_0$.

For Phase 1:

$$\begin{aligned}\mathbf{x^1_s}(t_0) &= T^1_{CS}[\mathbf{x_c}(t_0),\ \mathbf{S}] \\ \mathbf{x^1_s}(t_1) &= \mathbf{\Phi_1}(t_1 - t_0)\mathbf{x^1_s}(t_0) + \mathbf{\Gamma_1}(t_1 - t_0)\mathbf{S} \\ \mathbf{x_c}(t_1) &= T^1_{SC}[\mathbf{x_c}(t_0),\ \mathbf{x^1_s}(t_1),\ \mathbf{S}]\end{aligned} \tag{3.70}$$

For Phase 2:

$$\begin{aligned}\mathbf{x^2_s}(t_1) &= T^2_{CS}[\mathbf{x_c}(t_1),\ \mathbf{S}] \\ \mathbf{x^2_s}(t_2) &= \mathbf{\Phi_2}(t_1 - t_0)\mathbf{x^2_s}(t_1) + \mathbf{\Gamma_2}(t_2 - t_1)\mathbf{S} \\ \mathbf{x_c}(t_2) &= T^2_{SC}[\mathbf{x_c}(t_1),\ \mathbf{x^2_s}(t_2),\ \mathbf{S}]\end{aligned}$$

Applying the periodicity condition to the canonical variables[6], we have $\mathbf{x_c}(t_2) = \mathbf{x_c}(t_0)$.

All the transformations applied in equation (3.70) are linear in $\mathbf{S}$ and $\mathbf{x_c}(t_0)$ the final result is expressible as a linear combination of $\mathbf{S}$ and $\mathbf{x_c}(t_0)$:

$$\mathbf{x_c}(t_2) = \mathbf{F}\mathbf{x_c}(t_0) + \mathbf{H}\mathbf{S} \tag{3.71}$$

[6]Since they are the only variables guaranteed to be continuous across phase boundaries

Where $\mathbf{F}$ and $\mathbf{G}$ are determined by appropriately chaining the transformations in equation (3.70). Thus:

$$\begin{aligned}(\mathbf{I}-\mathbf{F})\mathbf{x_c}(t_0) &= \mathbf{HS} \\ \mathbf{x_c}(t_0) &= (\mathbf{I}-\mathbf{F})^{-1}\mathbf{HS}\end{aligned} \tag{3.72}$$

In general for N_{PH} phases one can show the following:

$$\mathbf{x_c}(t_m) = \mathbf{T_1^m x_c}(t_0) + \mathbf{T_2^m S} \tag{3.73}$$

Where:

$$\begin{aligned}\mathbf{T_1^m} &= \left[\prod_{j=0}^{m-1} \boldsymbol{\alpha}^{\boldsymbol{m-j}}\right] \\ \mathbf{T_2^m} &= \left(\sum_{j=1}^{m}\left[\prod_{j=0}^{m-1} \boldsymbol{\alpha}^{\boldsymbol{m+j+1-i}}\right]\boldsymbol{\beta}^{\boldsymbol{j}}\right) \\ \boldsymbol{\alpha}^{\boldsymbol{j}} &= \mathbf{Q_{c,dead}^j} + \mathbf{Q_x^j \Phi^j M^j} \\ \boldsymbol{\beta}^{\boldsymbol{j}} &= \mathbf{Q_s^j} + \mathbf{Q_x^j \Phi^j N^j}\end{aligned} \tag{3.74}$$

Using $m = N_{PH}$ and $\mathbf{x_c}(t_{N_{PH}}) = \mathbf{x_c}(t_0)$ in equation (3.73) we can get:

$$\mathbf{x_c}(t_0) = (\mathbf{I} - \mathbf{T_1^{N_{PH}}})^{-1}\mathbf{T_2^{N_{PH}} S} \tag{3.75}$$

This last result, equation (3.75), is quite important. We are now able to determine the values of the canonical variables at *steady state*. By starting from these values we can perform a very small transient to get one cycle of the steady state. Since the steady state is periodic, all information is contained in one period. Thus all steady state parameters can be evaluated from this single period. We do not need a full transient simulation.

3.3.2 Procedure for Calculation of Steady State Parameters

Starting from the value of $\mathbf{x_c}(t_0)$ at steady state, which we have shown how to compute in section 3.3.1, we can calculate several important parameters: output impedance, efficiency and ripple. The steps are:

1. Starting from $\mathbf{x_c}(t_0)$ perform a transient simulation for one period and store the state variables for each phase.

2. Convert each phase state variables to MNA solution vectors and then obtain the input current $I_{in} = I(V_{in})$ and output voltage $V_{out} = V(I_{out})$.

Calculation of Conversion Ratio Setting the output current zero, compute the effective output voltage according to the chosen definition: minimum voltage or average voltage.

$$\begin{aligned} V_{out,eff} &= \frac{1}{T}\int_0^T V_{out}(t)dt \quad \text{OR} \\ &= \min_{[0,T]}(V_{out}(t)) \end{aligned} \tag{3.76}$$

Then:

$$M = V_{out,eff}/V_{in} \tag{3.77}$$

Calculation of Output Impedance Compute the effective output voltage using equation (3.76). Then:

$$R_{eq} = \frac{(MV_{in} - V_{out,eff})}{I_{out}} \tag{3.78}$$

Calculation of Efficiency Compute Efficiency using (Only conduction losses included):

$$\eta = \int_0^T \frac{V_{out}(t)I_{out}}{V_{in}I_{in}(t)}dt \tag{3.79}$$

Calculation of Ripple

$$V_{Rip} = \max_{[0,T]}(V_{out}(t)) - \min_{[0,T]}(V_{out}(t)) \tag{3.80}$$

3.3.3 Computer Implementation

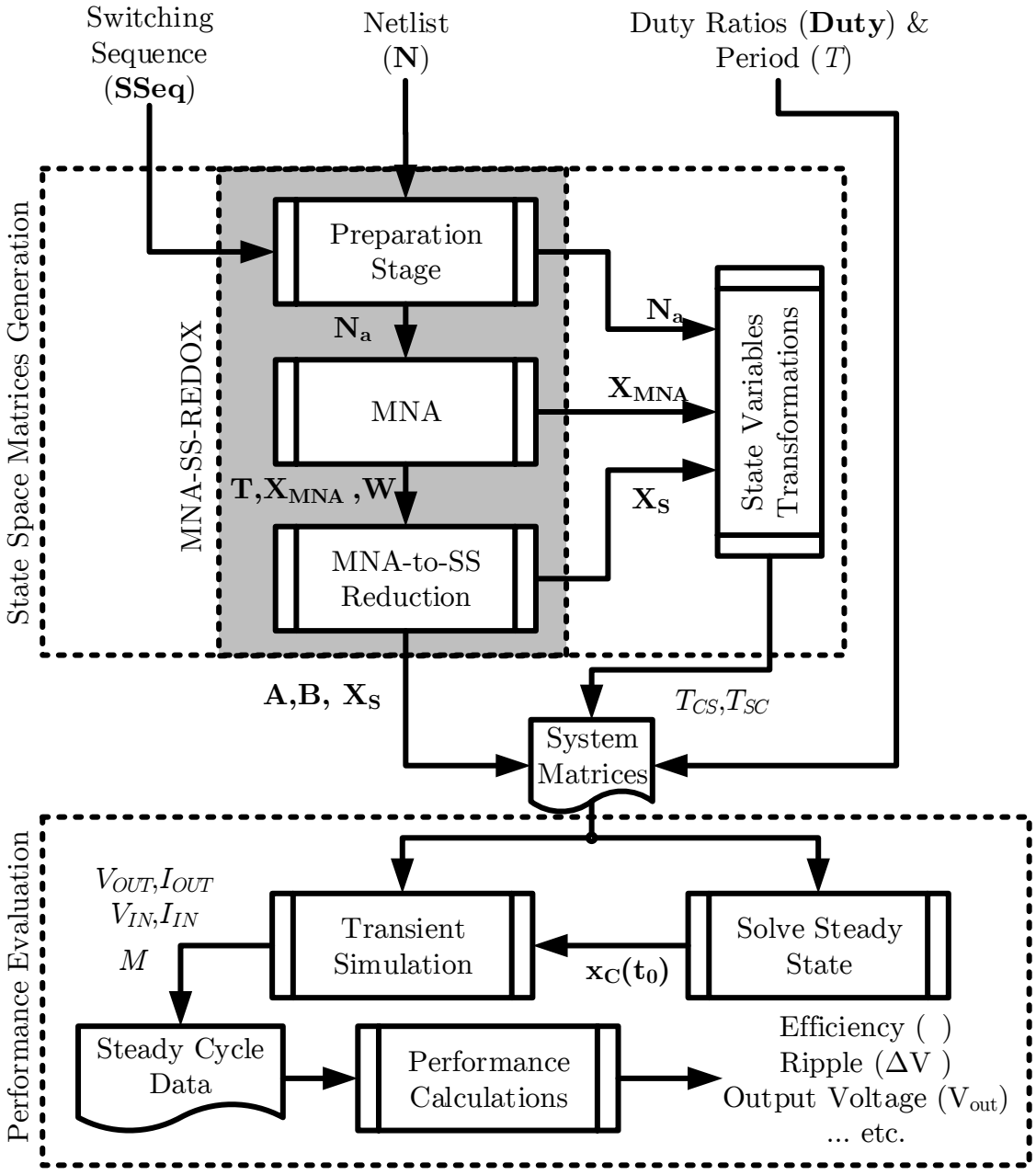


Figure 3.3: Data flow in the proposed algrotihm

Figure 3.3 shows the flow of data between the various parts of the proposed algorithm.

3.4 Verifcation

A proof of concept implementation of this algorithm was done in MATLAB to verify the algorithm. Two versions of the algorithm were implemented: a symbolic version and a numeric version. The symbolic version generates a step-by-step output of the intermediate matrices that are used to calculate the state space matrices and transformation matrices. The symbolic outputs were verified manually for some relatively simple cases. A sample of the output is shown in the Appendix .

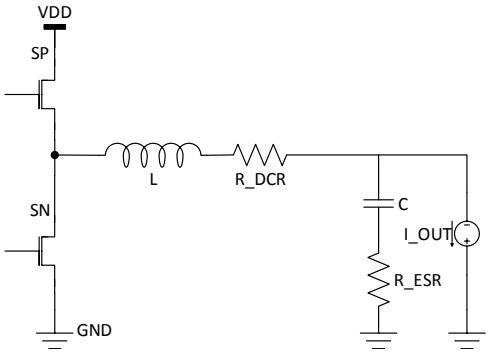
The numeric version was used as to evaluate the performance of several circuits. The generated results were compared against results generated from LTSpiceIV. The rest of this section examines this comparison.

The first test case is shown in Figure 3.4a. The inputs provided to LTSpiceIV and MNA-SS-REDOX are shown in Figure 3.4. The values of the components are: $V_{in} = 10V, L = 10\mu H, C = 100\mu F, R_{on} = 1\Omega, R_{DCR} = 1m\Omega, R_{ESR} = 1m\Omega$ and I_{out} is swept from 10mA to 1A.

The simulated time for LTSpiceIV is 3ms to ensure that steady state is reached. The efficiency is calculated and comapred to the MNA-SS-REDOX results.The overlap time (10ns) of the switches i.e. shoot through losses, was accounted for by including a small period with both switches ON in the switching sequence (as shown in Figure 3.4b). Figure 3.5 (a,b and c) show a comparison between the results from MNA-SS-REDOX and LTSpiceIV for efficiency, ripple and output voltage respectively. The results show good agreement ($\leq 1.3\%$ error) between MNA-SS-REDOX and LTSpiceIV. Note that in this case the duty was fixed at 0.4 which simulates an open loop converter.

Consider now the case where a designer who still has not designed his converter wants to evaluate the performance over the load range for a *specific* output voltage call it V_{REF}. This is a more realistic case. In this case the designer can run a 2D parametric sweep to determine which duties and load current pairs give the desired output voltage. The results of this sweep can be seen in Figure 3.6. The points equal to (or close) to desired voltage can be extracted and plotted as in Figure 3.7 for $V_{REF} = 4V$. From

this line a polynomial fit can be performed to determine the relation between load current and duty. In this case the algorithm generates $D = 0.3992 + 0.0995I_{Load}$. This is extremely close to the theoretical approximation $D = 0.4 + 0.1I_{Load}$. Now the designer can use this “control law" to run a sweep to determine the efficiency at $V_{out} = V_{REF} = 4V$. The results from MNA-SS-REDOX and LTSpice are shown in Figure 3.8



(a) Buck convertr with resistive parasitics for filter elements. Element names correspond to theose in netlists

```
V1 Vin 0 10
L1 Vx N001 10u
C1 Vout N002 100u
V2 Pctrl 0 PULSE(0 1 0 10n 10n 2u 5u)
V3 Nctrl 0 PULSE(0 1 2.u 10n 10n 3u 5u)
SP1 0 Vx Nctrl 0 mysw
SP2 Vx Vin Pctrl 0 mysw
Rdcr N001 Vout 0.001
Resr N002 0 0.001
I1 Vout 0 {ILoad}
.tran 0 3.02m 3m
.model mysw sw(Ron=1, Roff=100Meg, Vt=0.5, Vh = 0.4)
.meas Pout AVG(V(vout)*I(I1))
.meas Pin AVG(V(vin)*I(V1))
.meas VoutMax MAX(v(vout))
.meas VoutMin MIN(v(vout))
.meas VoutAvg AVG(v(vout))
.meas tran Eff PARAM 100*(Pout/Pin)
.meas tran Ripple PARAM VoutMax VoutMin
.STEP PARAM ILoad 0.01 1 0.034137931034482
.backanno
.end
```

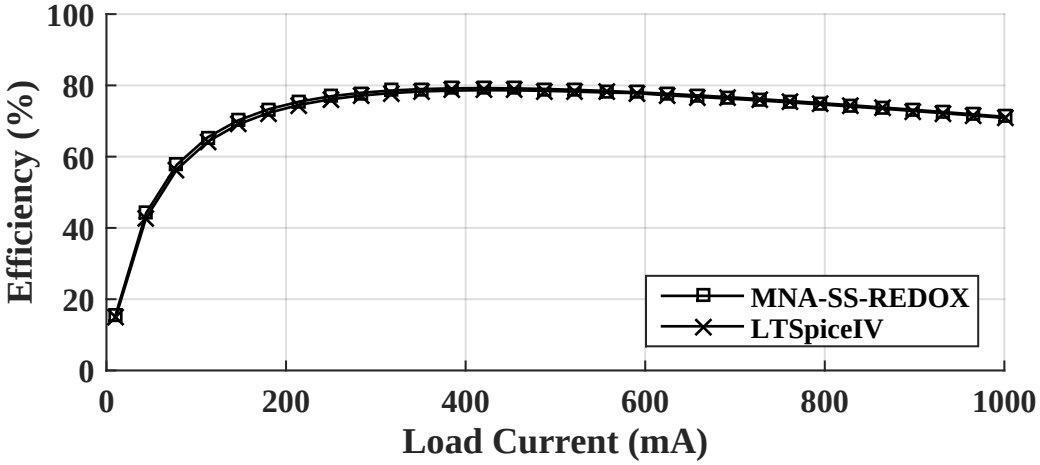
(b) LTSpiceIV Netlist used ofr simple buck converter

```
%% INPUTS
% NETLIST
N = {
{'V_in'      1    0};
{'I_out'     2    0};
{'S_P'       1    3};
{'S_N'       3    0};
{'L'         2    4};
{'R_dcr'     4    3};
{'C'         2    5};
{'R_esr'     5    0};
};
% Switching Sequence
SSeq = [
    1    0;
    1    1;
    0    1
];
```

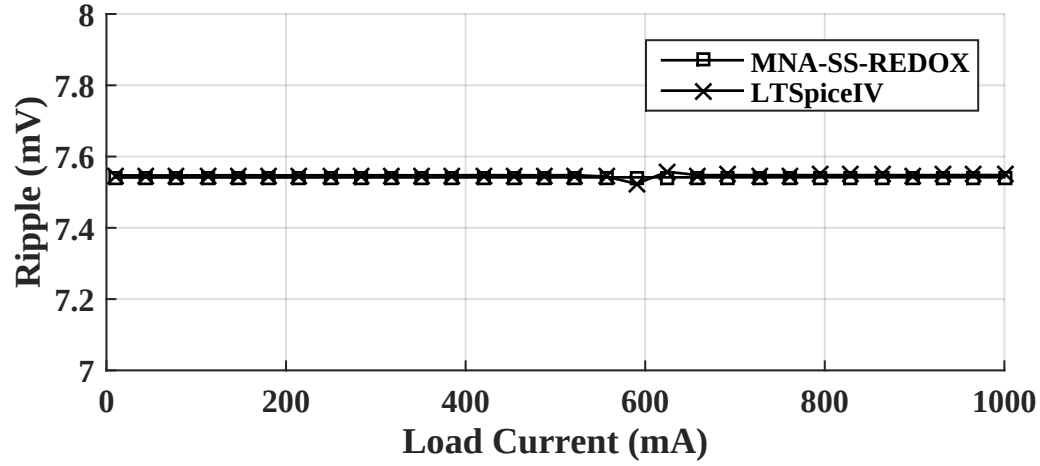
```
% Duty Ratios
syms D
Duty = [D   0.002 (1   D   0.002)];

% VARIABLE VALUES
syms L C
Vals = {
    'T'         0.5e 5;
    'D'         (0.4 + 0.1*sym('I_out'));
    'V_in'      10;
    'I_out'     logspace(2, 0, 30);
    'R_P'       1;
    'R_N'       1;
    'L'         10e 6;
    'R_dcr'     0.001;
    'C'         10e 5;
    'R_esr'     0.001;
};
```

(c) MATLAB input provided to MNA-SS-REDOX algorithm

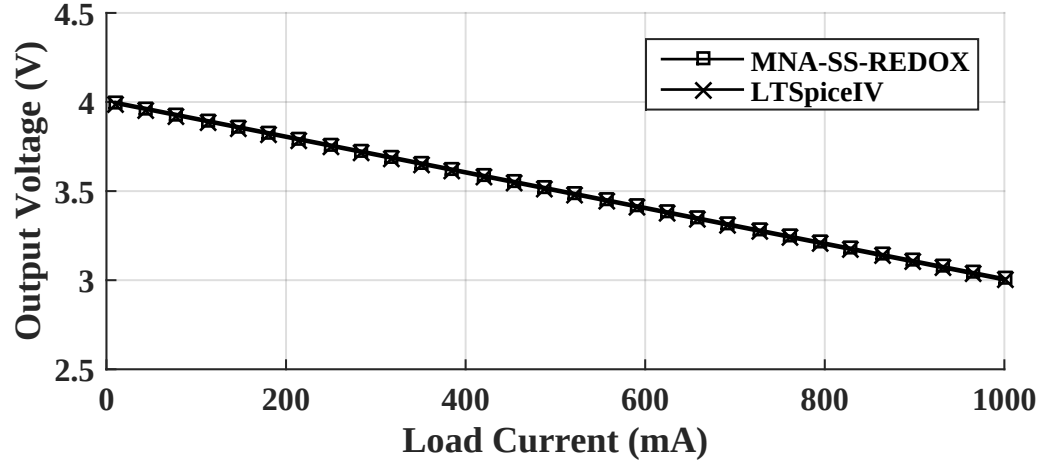
Figure 3.4: Verification Example 1: Simple Buck Converter



(a) Efficiency



(b) Ripple



(c) Output Voltage

Figure 3.5: Comparison of Simple Buck Converter Results from MNA-SS-REDOX and LTSpiceIV in Open Loop

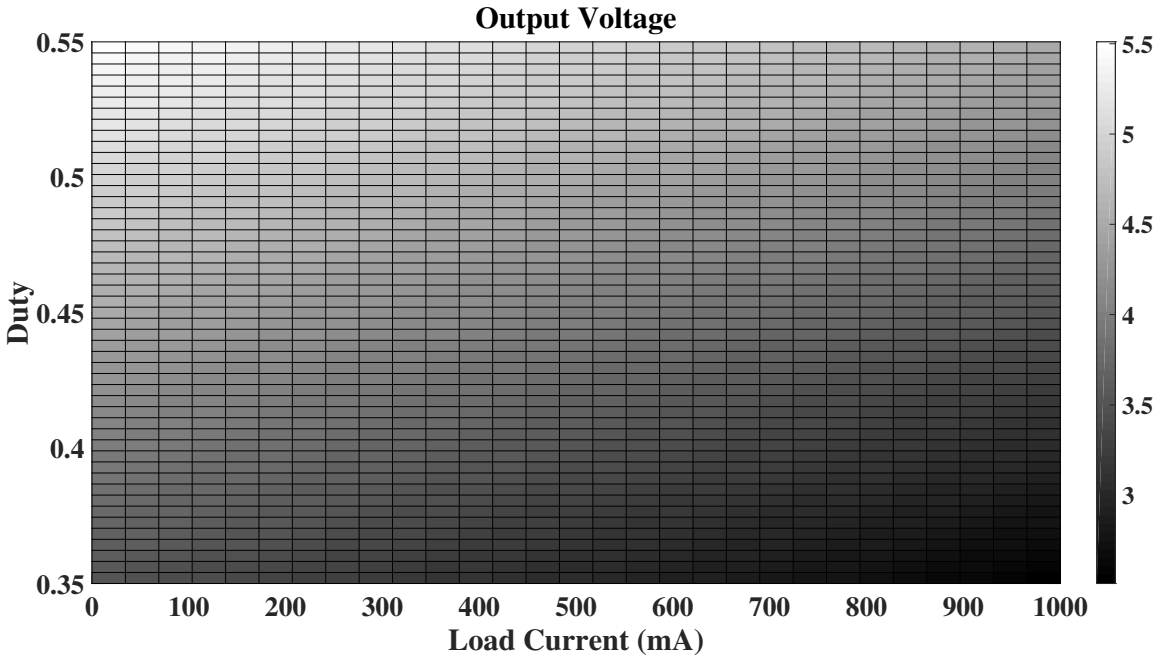


Figure 3.6: Output voltage as a function of load current and duty ratio

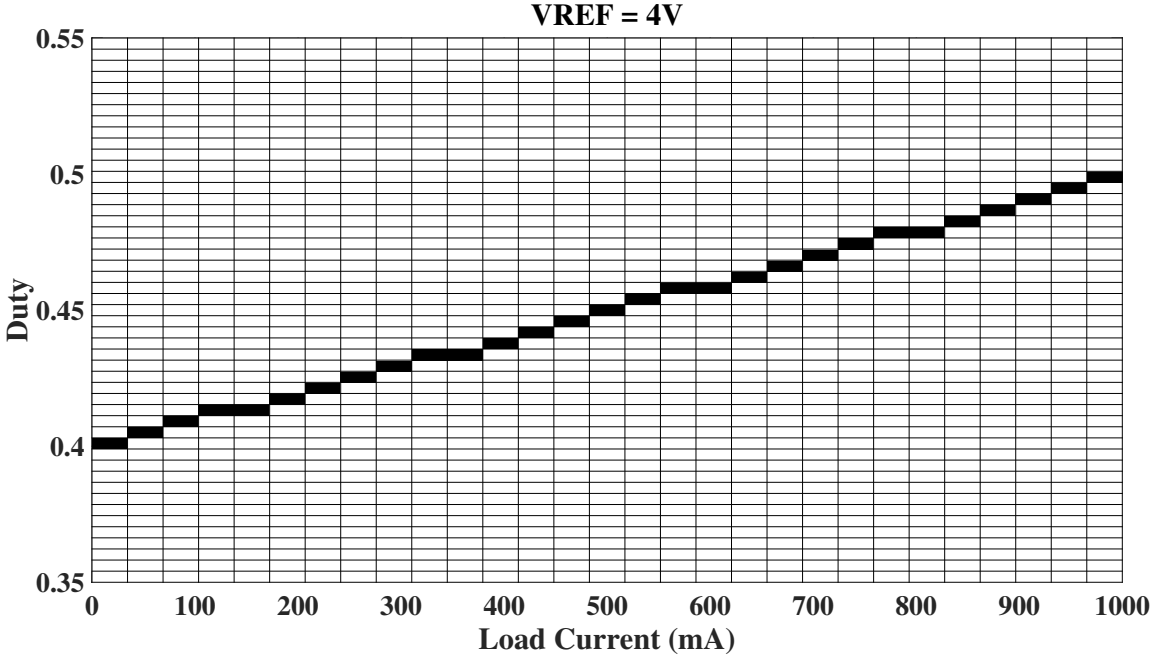
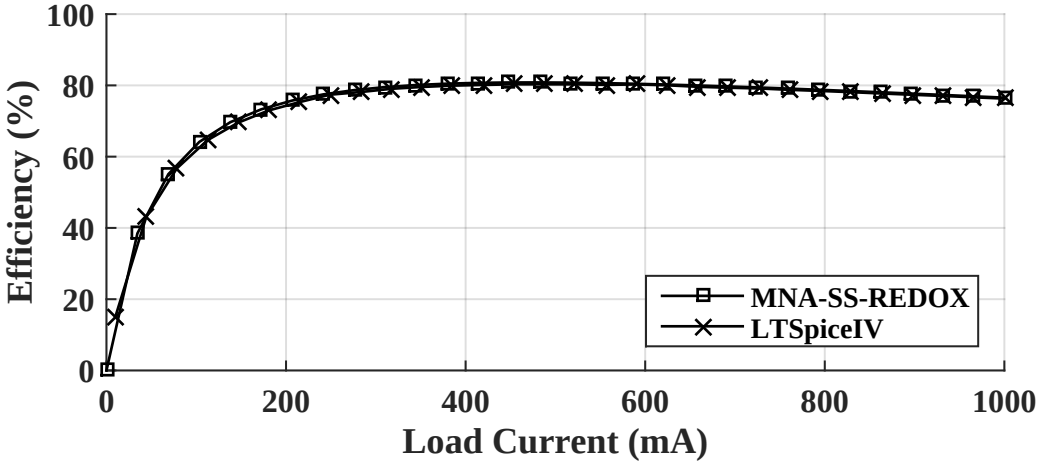
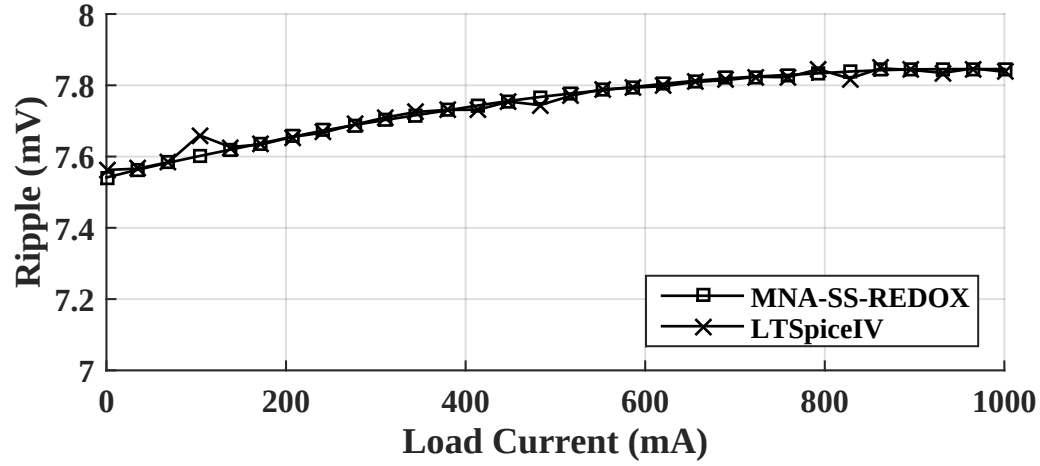


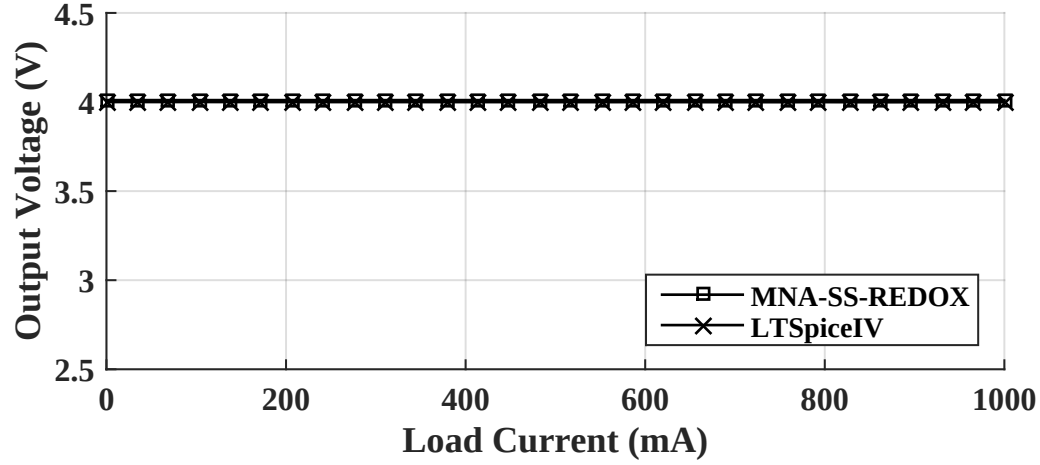
Figure 3.7: Each black point represents a Load Duty pair for which $V_{out} = V_{REF} = 4$



(a) Efficiency



(b) Ripple



(c) Output Voltage

Figure 3.8: Comparison of Simple Buck Converter Results from MNA-SS-REDOX and LTSpiceIV regulated by $D = 0.4 + 0.1I_{Load}$

CHAPTER 4

SWITCHED CAPACITOR CONVERTER DESIGN AND SIMULATIONS

4.1 Overall Diagram

In designing the SCC converter there are several decisions to be made. We have already decided on power stage. What remains are the sizing of the power stage and control mechanism. SCC converters as discussed previously have several control methods. However the simplest and most widely adopted are the frequency based control methods. Pulse skipping and PFM are the main methods.

Pulse Skipping is simpler to implement and usually has faster transient response. On the other hand PFM has less ripple in the output and has potential for higher efficiency since all parts of the circuit including control can be scaled in frequency. PFM also needs special attention to stability.

In this chapter we will implement PFM. The overall diagram of the SCC converter is shown in Figure 4.1. The diagram shows the PFM system. The comparator signals the charge pump to increase or decrease the VCO frequency according to whether the output voltage is higher or lower than the reference. To use pulse skipping we disconnect the VCO from the decoders and connect signal BL in its place. The comparator should be clocked by the maximum expected power stage frequency.

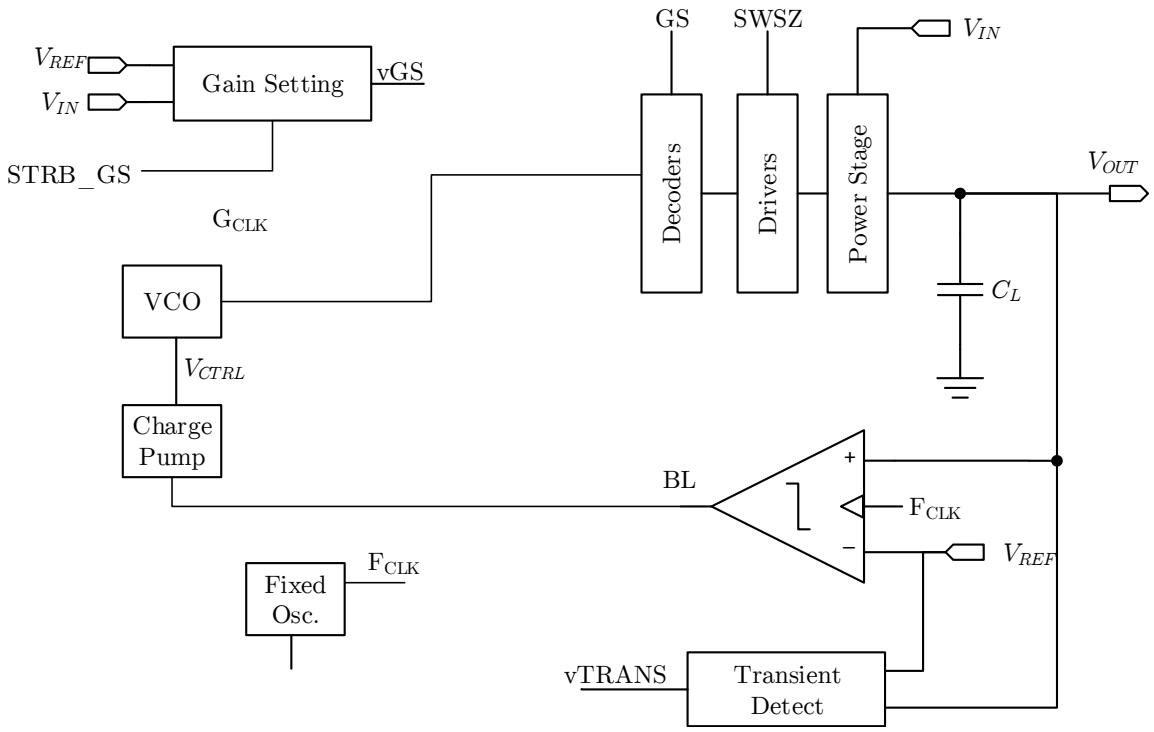


Figure 4.1: SCC Converter ovrall block diagram

To implement this system one needs design the individual components and ensure their interoperation. We start by selecting and sizing the power stage components section 4.2. We next describe the decoders and drivers section 4.3. We then propose a supply insensitive voltage controlled oscillator(VCO) for our application section 4.4. The three sensing units (gain setting unit, transient detector and reference comparator) are presented. Finally some simulation results are presented section 4.7.

Notice that in section 4.2 we will not be using our the proposed design methodology since it is incomplete yet.

4.2 Power Stage

The power stage of an SCC converter consists of capacitors and switches. The majority of the area will be occupied by capacitors. Hence it is important to use the highest density capacitors available. There are several options of capacitors available as shown in table 4.1. The metal finger optio is not an intrinsic option in the technology rather

Table 4.1: Capacitor Device options in the $LF150nm$ technology

Device Type	Capacitance Density ($fF/\mu m^2$)
Thin Oxide `nmos1v8hvt`	9.4
Thick Oxide `nmos3v3hvt`	4.8
MIM	0.98
Metal Finger	1.5

is is formed by using metal layers with interdigitated metal fingers as descibed in [56]. We used three metal layers (METAL2- METAL4). The highest density seems to be the `nmos1v8hvt` derived capacitor (9.4 fF/μm). As such we will use this as our default choice.

For the switches the thinner oxide alternatives have higher trans-conductivity parameters and hence lower resistance. We will also use minimal length transistors. The type of switch used depends on its location in the power stage. For switches connected to the supply we will PMOS, NMOS for ground connected switches and for tranns-mission gates (TGATES) for output or intermediate node connected switches. The diagram of the power stage with approprate switches is shown in

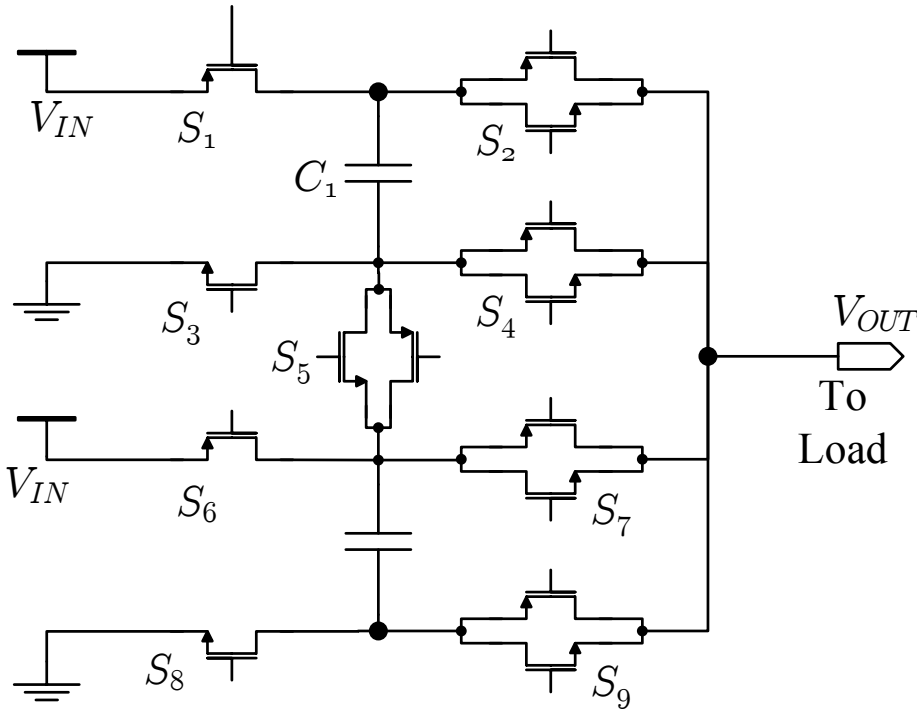


Figure 4.2: Single Phase of Power Stage with switch types specified.

Capacitor Sizing The converter must sustain a maximum load of 5mA (chosen arbitrarily). At SSL limit the current driving capability of the converter is given by:

$$I_L = N_{caps} f C_T V_{Diff} \tag{4.1}$$

where

$$V_{Diff} = V_{in} - V_{out} \tag{4.2}$$

Assume we operate at a frequency of about 10MHz. We have 3 phases with 2 capacitors each. Assume a V_{Diff} of 200mV. Then we have:

$$C_T = I_L/(N_{caps} f V_{Diff}) = 416\text{pF} \tag{4.3}$$

Using the capacitance density we can compute the area required as about 450μm$\times$ 100μm.

Switch Sizing To calculate the switch resistances we assume that we can charge the capacitor fully in half cycle. This means the charge time constant $3\tau = 3RC$ (which gives 95%) must be:

$$\begin{aligned} 3\tau = 3RC = 3(2R_{sw})C \leq 1/(2f) \\ R \leq 1/(12fC) = 20\Omega \end{aligned} \tag{4.4}$$

Next we need to characterize the MOSFETs we will use as switches. The circuit used to characterize the MOSFET connects two sources VGS and VDS to the gate and drain respectively. The source and bulk are grounded. We seek to find for a given width W_0 what are the unit resistance and gate capacitance R_0 and C_0. Note that we are using to fingers of 5μm each to give 10μm total; at minimum length.

The capacitance and resistance as functions of V_{GS} are shown in Figure 4.3. The minimum resistance at $V_{GS} = 1.8$V is 68.3Ω. The maximum capacitance is around 15fF. The PMOS has a minimum resistance of 216Ω with a capacitance of 15fF. The switch widths are found to be 35μm for NMOS and 108 μm for PMOS.

From these values power stage switching losses at the nominal frequency of 10MHz can be evaluated. Each gain setting has a different combination of switches working. The losses turn out to be:

$$\text{Gain Setting } (1/1) = 24.3146\mu\text{W}$$
$$\text{Gain Setting } (2/3) = 34.5425\mu\text{W}$$
$$\text{Gain Setting } (1/2) = 38.1316\mu\text{W}$$
$$\text{Gain Setting } (1/3) = 46.6997\mu\text{W}$$

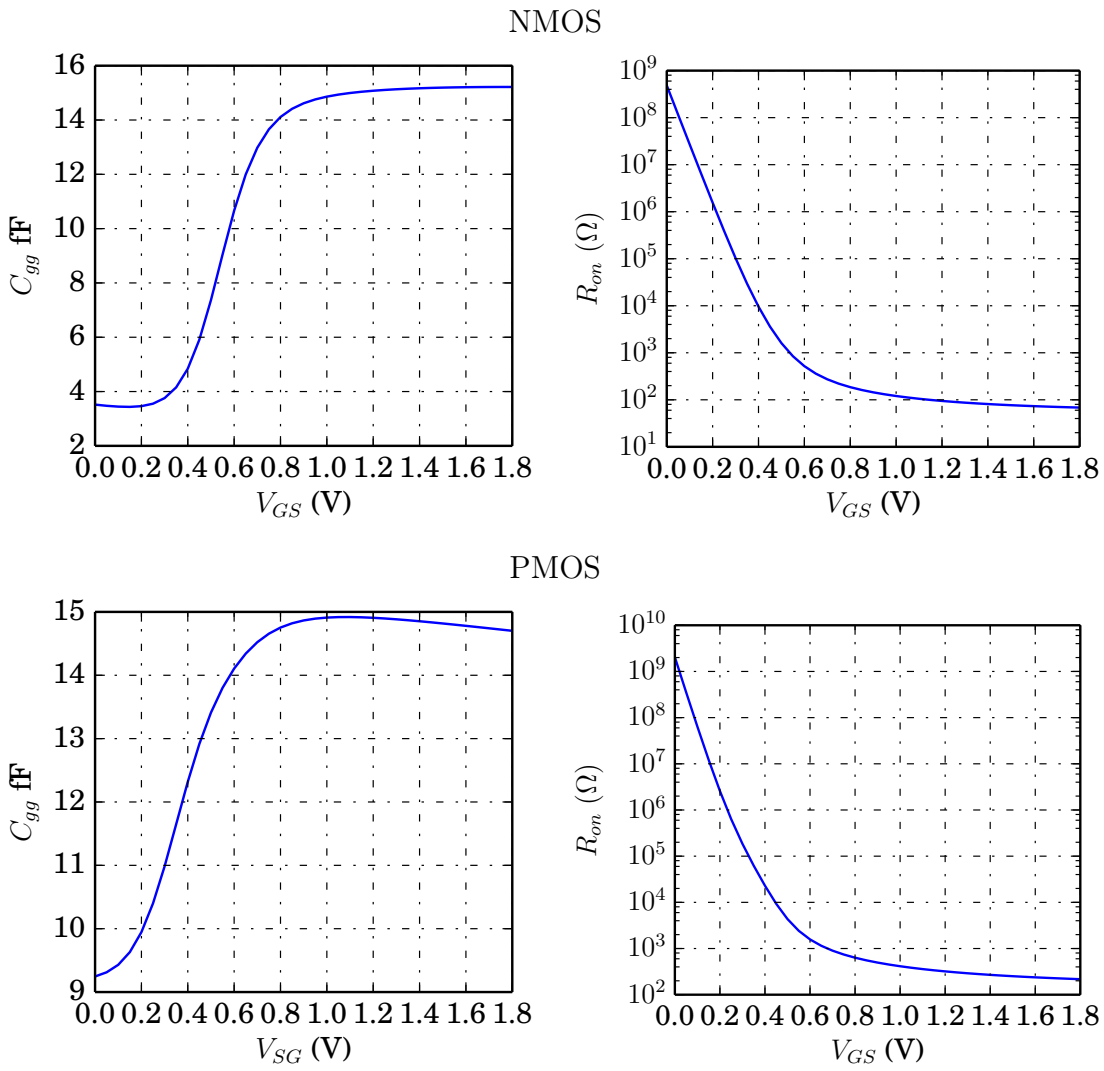


Figure 4.3: Graph of Gate capacitance and channel resistance for NMOS and PMOS in LF150nm technology

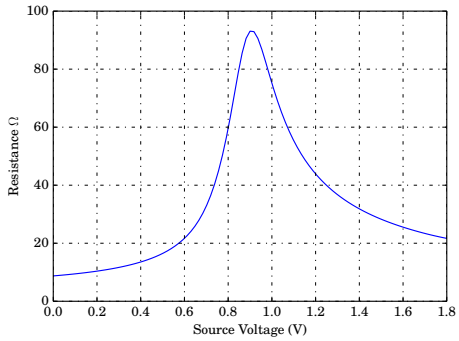


Figure 4.4: Resistance of transmission gate as source voltage varies.

4.3 Decoders and Drivers

The decoder has four inputs GS<0:1>, SWSZ<0:1>, Phi1 and Phi2. There are two outputs: SWN<1:27> and SWP<1:27>. The decoder was described using Verilog code shown in Figure 4.5. This is synthesized using RTL Compiler (RC).

Two inverters are used as buffers for switches larger than 40 μm.

```
//Verilog HDL for "SCC", "drv_decoder" "verilog"


module drv_decoder (SWN, SWP, GS, Phi1, Phi2, SWSZ );
    input   [0:1] GS;
    input   [0:1] SWSZ;
    input   Phi1;
    input   Phi2;

    output  [1:27]  SWN;
    output  [1:27]  SWP;

    assign SWN[1:9] =
/*gss*/ (               //~SW1,  SW2,  SW3,  SW4,  SW5,  ~SW6,  SW7,  SW8,  SW9
/*1/3*/ (GS == 2'b11) ? ({Phi1, Phi2, Phi2, 1'b0, Phi1, 1'b0, Phi2, Phi2, Phi1}) :
/*1/2*/ (GS == 2'b10) ? ({Phi1, Phi2, Phi2, Phi1, 1'b0, Phi2, Phi1, Phi1, Phi2}) :
/*2/3*/ (GS == 2'b01) ? ({Phi1, Phi2, 1'b0, Phi1, Phi2, Phi1, 1'b0, Phi2, Phi1}) :
/*1/1*/ (GS == 2'b00) ? ({Phi1, Phi2, 1'b1, 1'b0, 1'b0, Phi2, Phi1, 1'b1, 1'b0}) :
/*xyz*/                 ({1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0})
    );

    assign SWP[1:9] = ~
/*gss*/ (               //SW1,  SW2,  SW3,  SW4,  SW5,  SW6,  SW7,  SW8,  SW9
/*1/3*/ (GS == 2'b11) ? ({Phi1, Phi2, Phi2, 1'b0, Phi1, 1'b0, Phi2, Phi2, Phi1}) :
/*1/2*/ (GS == 2'b10) ? ({Phi1, Phi2, Phi2, Phi1, 1'b0, Phi2, Phi1, Phi1, Phi2}) :
/*2/3*/ (GS == 2'b01) ? ({Phi1, Phi2, 1'b0, Phi1, Phi2, Phi1, 1'b0, Phi2, Phi1}) :
/*1/1*/ (GS == 2'b00) ? ({Phi1, Phi2, 1'b1, 1'b0, 1'b0, Phi2, Phi1, 1'b1, 1'b0}) :
/*xyz*/                 ({1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0})
    );

    assign SWN[10:18] = ((SWSZ > 0) && (SWSZ < 3)) ? //SWSZ = 00
                    (SWN[1:9]) :
                    {1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0};

    assign SWN[19:27] = ((SWSZ > 1) && (SWSZ < 3)) ?
                    (SWN[1:9]) :
                    {1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0, 1'b0};

    assign SWP[10:18] = ((SWSZ > 0) && (SWSZ < 3)) ? //SWSZ = 00
                    (SWP[1:9]) :
                    {1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1};

    assign SWP[19:27] = ((SWSZ > 1) && (SWSZ < 3)) ?
                    (SWP[1:9]) :
                    {1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1, 1'b1};

endmodule
```

Figure 4.5: Decoder Code listing

4.4 Voltage Controlled Oscillator[1]

The optimum frequency of operation depends on balancing load independent switching losses and linearly varying with load conduction losses. The optimal frequency varies with load, [36]. Hence, a controlled oscillator is desirable to maximize conversion efficiency for different loading conditions.

The oscillator drives decoding circuitry that provide switching signals, these are buffered by the drivers and applied to switches in the power stage. A common technique traditionally applied to reduce the input and output ripple is using multiple phases in the power stage [36]. This requires that the oscillator be able to provide multiphase signals. It is desirable that the output of the oscillator have sharp edges (small rise and fall times) and rail-to-rail characteristics to cause abrupt switching and properly drive the non-overlapping clock generators to avoid shoot-through power loss. Converters usually have variable or unregulated inputs. Strong dependence of oscillation frequency on supply voltage forces the designer to use a separate small regulator for the oscillator which increases overhead and design time. Some of the recent works reporting switched capacitor converters either employ a separate regulator [37], or use external clocks [10, 71] which are impractical in self-contained systems.

4.4.1 Analysis of Cross Coupled Inverter based Delay Cell

A ring oscillator with N stages and T_D delay per stage has an oscillation frequency of $f_{osc} = 1/2NT_D$. For delay elements with different rise and fall times, the delay is evaluated as the average, i.e. $T_D = 0.5(T_{LH} + T_{HL})$ [72]. Figure 4.6 shows a three phase ring oscillator. We will later use the delay cell to implement it.

Consider the delay cell reported in [73] shown in Figure 4.7. The inputs are nodes A, B and CTRL with voltages V_A, V_B and V_{CTRL} respectively. The outputs are nodes AY and BY with voltages V_{AY} and V_{BY}. Let V_A and V_B be complementary clock signals i.e. when $V_A = V_{DD}$, $V_B = 0$ and vice versa. The current through NC charges (or discharges) node BY to V_{TN} (or $V_{DD} - V_{TP}$) where the positive feedback action

[1]This section is largely the material of a paper accepted for NEWCAS 2015

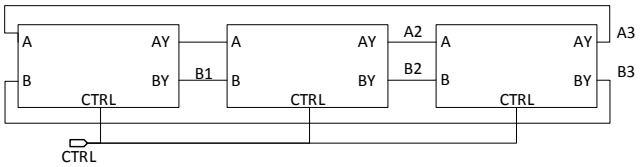


Figure 4.6: Block Diagram Three phase ring oscillator

of the cross coupled latch formed by NA, PA, NB and PB takes over and quickly switches V_{BY} to the other state. The current paths are shown in Figure 4.8. A typical wave form in this case is shown in Figure 4.9. The analysis can be divided into three regions: two for low to high and one for high to low.

Consider the high to low transition first (marked A in Figure 4.9). $V_A = 0, V_{BY} = V_{DD}$. Through NC, node A discharges node BY down from V_{DD} to $V_{DD} - V_{TP}$. Since NC is an NMOS transistor A is the source and BY is the drain. Assuming $V_{DD} - V_{TP}$ is sufficient to keep NC in saturation and ignoring the time for positive feedback action (usually in sub nanosecond range), we have:

$$T_{HL} = \frac{(C_{par} V_{TP})}{I_{avg,NC}} \tag{4.5}$$

The total parasitic capacitance at node BY is C_{par}, and $I_{avg,NC}$ is the average current through NC. This current will be almost constant if NC is long enough to minimize the effect of channel length modulation and hence minimize the effect of drain to source voltage. The drain to source voltage (between V_{DD} and $V_{DD} - V_{TP}$) is directly related to the supply. Hence minimizing its effect also minimizes the effect of the supply. Once BY reaches $V_{DD} - V_{TP}$ regenerative action quickly discharges BY to GND.

Consider now the low to high transition (composed of B and C in Figure 4.9). In this case it is more complicated. There are one or two regions depending on V_{CTRL} (assuming $V_{CTRL} > V_{TN}$). With $V_A = V_{DD}$ and initially $V_{BY} = 0$, node BY will be charged through NC (which is in saturation) (Region B in in Figure 4.9.) as it rises $V_{GS} = V_{CTRL} - V_{BY}$ might no longer be greater than the threshold of NC. In this case NC enters sub-threshold region and the current through NC becomes small. V_{BY} takes quite some time till reaches close to V_{TN} (Region C in in Figure 4.9.).

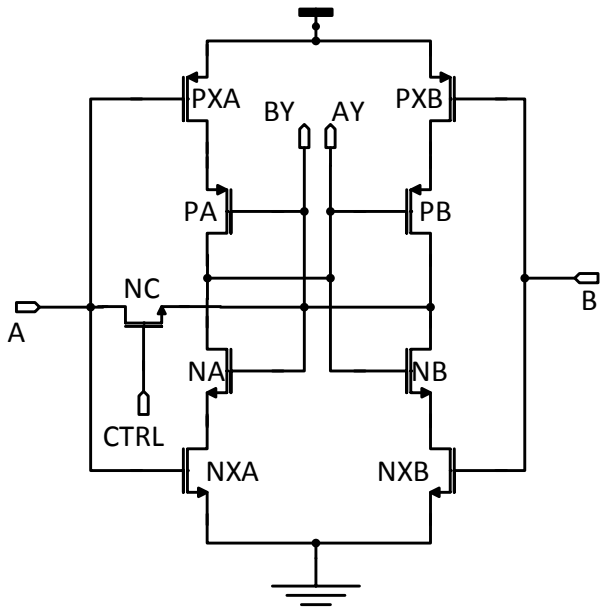


Figure 4.7: Circuit Diagram of Cross Coupled inverter based delay element

Otherwise, if $V_{CTRL} - V_{BY}$ is greater than V_{TN} before regenerative feedback starts i.e. $V_{CTRL} > 2V_{TN}$, then NC continues in saturation until regenerative action starts. If $V_{CTRL} < 2V_{TN}$ then the transistor enters sub-threshold. Again the delay is given by:

$$T_{LH} = (C_{par}V_{TN})/I_{avg,NC} \tag{4.6}$$

The current in sub-threshold mode, assuming large drain-source voltage is given by [74]:

$$I_D = I_0(e^{\frac{V_{GS}}{\zeta V_T}}) \tag{4.7}$$

Where I_0 and ζ are the current scale factor and non-ideality factor respectively. In saturation assuming negligible channel length modulation (long channel transistor) [74]:

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_{TN})^2 \tag{4.8}$$

Where μ, C_{ox}, W, L are the mobility, unit oxide capacitance, width and length respectively. The average current is some V_{CTRL} dependent combination of the saturation and sub-threshold currents. Notice that both expressions have no dependence on

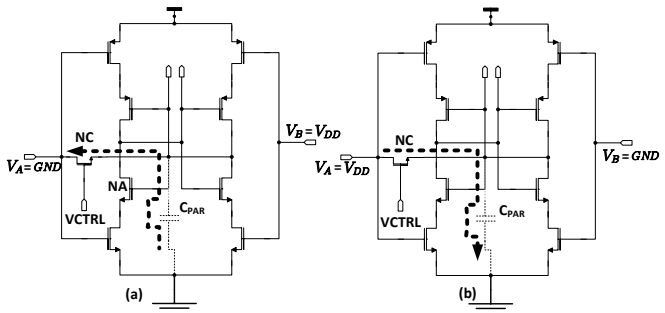


Figure 4.8: Charge(a) and discharge (b) current paths

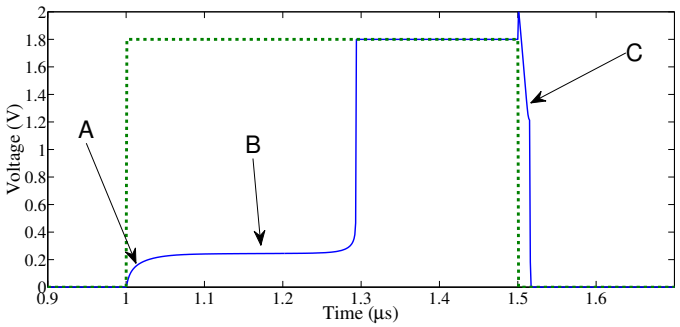


Figure 4.9: Typical Waveform showing charge and discharge of parasitic at BY (solid) for a square wave input (dot-dot)

drain to source voltage and hence no dependence on supply. Once V_{BY} reaches V_{TN} regenerative action of the latch starts and V_{BY} quickly develops to V_{DD}.

From the previous discussion we conclude that given V_{DD} sufficient to keep NC in saturation and that NC made with sufficiently long channel, then the delay is relatively independent of supply voltage. Consequently, an oscillator derived from this delay cell will also have an oscillation frequency that is relatively supply insensitive. Notice that V_{AY} and V_{BY} will be complementary signals.

4.4.2 Voltage Controlled Oscillator Simulation

To demonstrate the supply insensitivity a three phase ring oscillator i.e. three delay cell is designed in LF150nm technology. The sizing of the cross coupled inverter (NA, NB, PA, PB) is not important. As such we chose minimal size transistors for NA, NB for gate capacitance and hence minimal power. The sizing of an inverter (optimized for smallest delay) in LF150nm technology is 1.5 times larger for the PMOS. As such

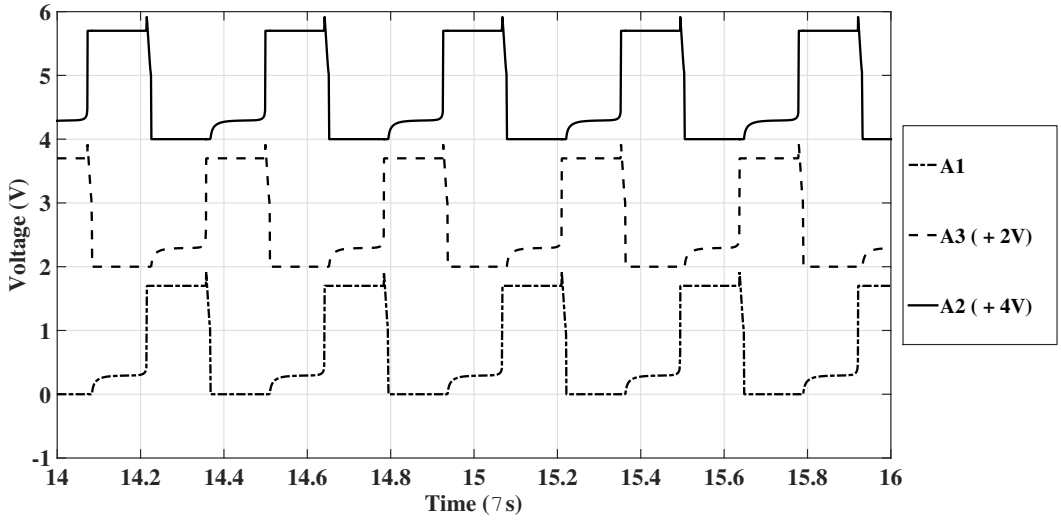


Figure 4.10: Typical oscillation waveform showing three phases. Output A1 Output A3 (shifted by 2V), and Output A2 (shifted by 4)

PA and PB were 1.5 times larger. The other transistors (PXA, PXB, NXA, and NXB) were made double the corresponding transistor (PA, PB, NA, and NB). NC must be made long enough to reduce channel length modulation. Since the currents depend on the length and hence the frequency, the width was fixed at minimal width and optimized the length for the desired range of frequencies (this is discussed later). The length is 5 μm.

A typical oscillation waveform showing the three outputs is shown in in Figure 4.10. (The waveforms for A2 and A3 are offset by 2 V and 4 V respectively for clarity). The variation of oscillation frequency as V_{DD} varies from 1.2 V to 1.8 V for various values of V_{CTRL} is shown in in Figure 4.11. As can be seen there is little variation with V_{DD} proving the supply insensitivity. The upper trace (V_{CTRL} = 1.2 V) shows some curvature, i.e. variation with V_{DD} when V_{DD} is close to 1.2 V. With V_{CTRL} = 1.2 V the transistor is close to the edge of saturation and hence more responsive to V_{DD} changes. The power consumption and frequency of oscillation as functions of V_{CTRL} for V_{DD} = 1.8 V are shown in Fig. 8. As expected the power consumption follows frequency in the absence of supply voltage variation. The circuit consumes little power (360 nW at 2 MHz, 13 μW at 66.68 MHz).

The current in NC decreases as the length of NC increases and thus we expect

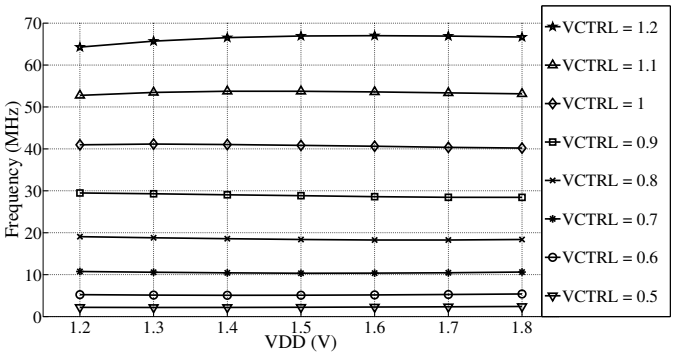


Figure 4.11: : Frequency of oscillation as a function of VDD for different VCTRL values. Upper trace is VCTRL = 1.2 V while lower trace is VCTRL = 0.5 V.

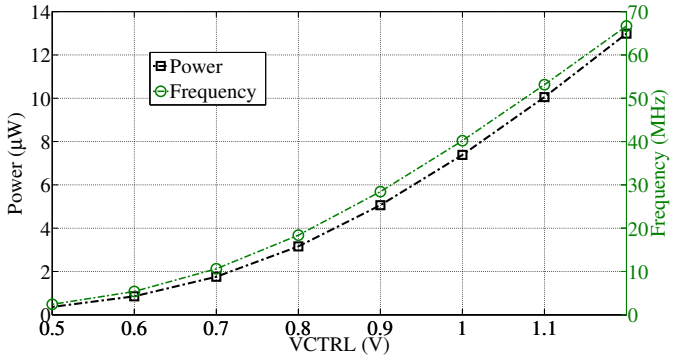


Figure 4.12: Power consumption (Left-axis, square) and Frequency (Rigth axis, circle) vs. Control voltage for 1.8V supply

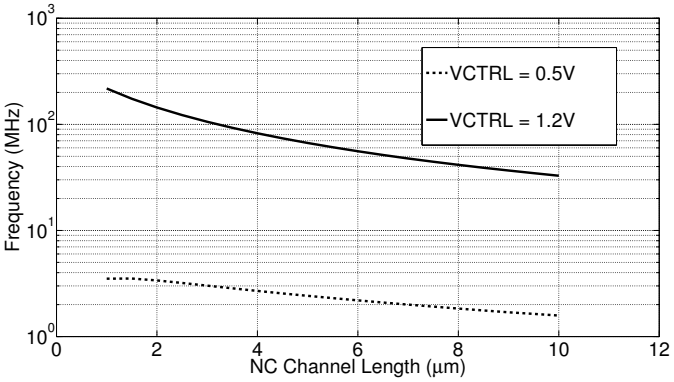


Figure 4.13: Variation of minimum frequency (VCTRL = 0.5) and maximum frequency (VCTRL = 1.2) with NC's channel length. Logarithmic scale used for frequency

the frequency to decrease. The exact choice of length depends on the range of desired frequencies, the control voltage range and the margin of technology variation allowed. For demonstration assume we need a tuning range of 3 to 50 MHz, for a control

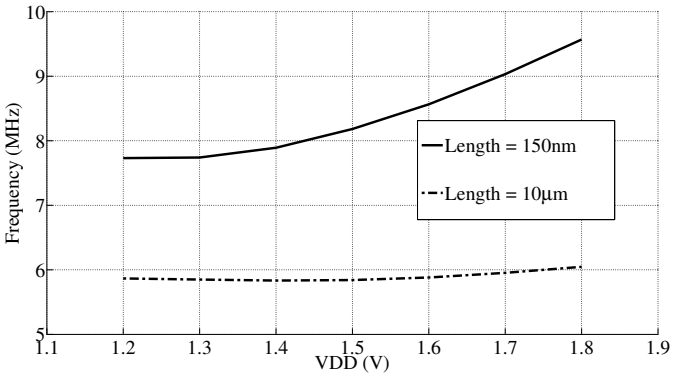


Figure 4.14: Variation of frequency with supply voltage for two length values: $150nm$ and $10\mu m$

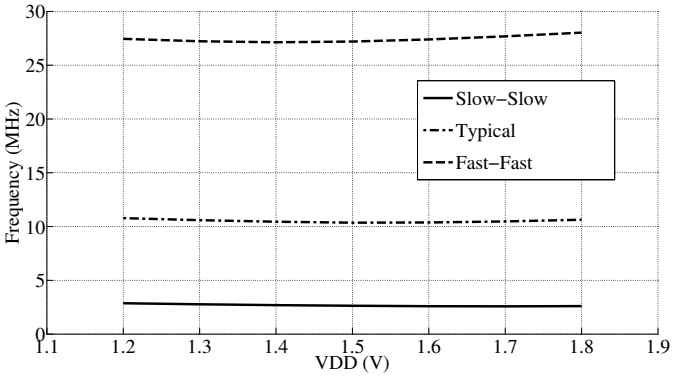


Figure 4.15: Variation of frequency with supply voltage for different technology corners: fast-fast, typical and slow-slow.

voltage range of 0.5 to 1.2 V. The variation of maximum frequency (V_{CTRL} = 1.2 V) and minimum frequency (V_{CTRL} = 0.5 V) as a function of length is shown in Fig. 4.13. At $5\mu m$ length the minimum frequency is 2.4 MHz and the maximum is 65 MHz which satisfies our range and leaves a margin of 15 MHz on the upper side. As will be seen in the corner analysis, different technology corners can decrease or increase the frequency three fold which may significantly narrow the available design range.

To verify that the increasing the length of NC does reduce sensitivity to supply, we sweep V_{DD} from 1.2 V to 1.8 V at a control voltage of 0.7 V. The results are shown in Fig. 4.14 For a length of 150 nm the frequency has a minimum of 7.7 M and a maximum of 9.5 MHz. With the length increased up to $10\mu m$ the minimum and maximum are 5.83 MHz and 6.05 MHz respectively i.e. less variation.

The analysis in previous section shows delays have direct dependence on technology

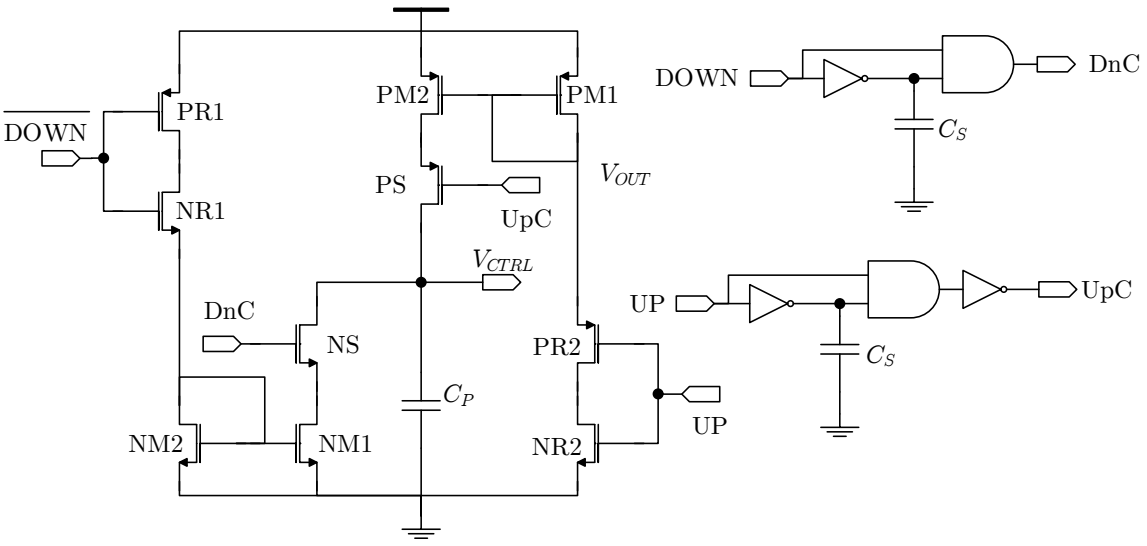


Figure 4.16: Charge pump used to control VCO

parameters such as the threshold voltages of the NMOS and PMOS. A corner sweep was performed to see the effect of variation on the sensitivity to supply voltage. The results are in Fig. 4.15. As expected there is a large change of frequency. For $V_{CTRL} = 0.7V$ the slow-slow corner produces 2.7 MHz while the fast-fast corner produces 27 MHz. This however should not cause an issue. The VCO will be part of a negative feedback loop that will set the frequency appropriately. A disadvantage however is the increase of voltage swing requirement for the circuit driving the VCO (the charge pump in this case).

4.5 Charge Pump

A circuit diagram of the charge pump we will be using is shown in Figure 4.16 This charge pump si very similar to that employed in [73]. The output voltage V_{CTRL} is across the capacitor C_P. NR1, PR1 and NR2 PR2, form resistors when UP or DOWN are applied. They set the currents flowing through the mirrors NM1, NM2 and PM1, PM2. The mirror currents pass only for a very short interval determined by the width of the pulse on UpC and DnC. These pulses are in turn determined by the values of C_S. The circuits producing UpC and DnC are simply edge detectors that detect the

rising edges of the UP and DOWN signals respectively. These determine how much charge is deposited on C_P per pulse of UP or DOWN.

Since the charge pump accumulates charge over time it can be considered as an integrator. From a small signal analysis perspective the amount of charge deposited on C_P per pulse is similar to the gain of an integrator. This makes it critical to the stability of the system. A large gain can cause large overshoots in frequency or even altogether instability. Too small gain can cause very long settling times.

4.6 Sensing

In the architecture used here there are three functions for sensing: determining the correct gain setting, checking whether the output is above or below the reference and determining if the output has exceeded the transient bounds ($\pm\Delta$) from the reference.

Reference Comparison

This is simply a comparator that compares whether the output voltage is higher or lower. The output BL signal is LOGIC 1 when the output is lower. A clocked comparator is most suitable for this because its power consumption scales with the frequency of clocking. The clocked comparator also renders a decision quickly. There are many dynamic comparators discussed in the literature. [37, 75–78]. Strong ARM comparator is one of the most commonly used. It is shown in Figure 4.17a. Goll and Zimmerman in [75, 76] propose improvements to lower the necessary supply voltage, this is shown in Figure 4.17b. A slight issue with these comparators is the metastability that happens when the inputs are below the threshold range. To alleviate this issues we modify the Goll-Zimmerman latch by adding a second parallel input stage such that the comparator becomes rail to rail. This is shown in Figure 4.17c.

Gain Setting

To determine which gain setting to use a potential divider ladder of metal layer resistor (total of about 1K) is used. To avoid large curretnts that will flow in such a small

resistance if it was continuously ON, we use a footer transistor [37]. The ladder is followed by a set of comparators that compare the reference voltage V_{REF} with several ratios of the input voltage V_{IN}. In our case these signals are $2V_{IN}/3 - \delta$, $V_{IN}/2 - \delta$ and $V_{IN}/3 - \delta$. δ is a small offset voltage. It accounts for the fact that at the nominal voltage of a gain setting, the converter can provide no current. Hence voltages near a gain settings nominal voltage must not be included in the range of load voltages it covers. The circuit is shown in Figure 4.18. The comparators are the same as those used in the Reference Comparator.

The circuit receives V_{IN}, V_{REF} and STRB_GS. From STRB_GS it generates two narrow pulses, STRB1 and STRB2. STRB2 is a delayed version of STRB1. STRB1 activates the ladder which due to its small resistance settles quickly at its final voltages. Once settled, STRB2 activates the comparators, whose output is latched (latches not shown). A full adder adds the values to obtain the vGS<0:1>. For example consider all the comparators gave a value of LOGIC 0, meaning the reference is higher than all divided versions of the input. In this case the output is 00 which indicates the 1/1 Gain Setting.

Two of these comparators are used. One is fed with $V_Y = V_{REF} - \Delta$ and the other with $V_Y = V_{REF} + \Delta$. The resulting signals, AUB and BLB indicate whether the output voltage V_{OUT} is above the upper bound (AUB) or below the lower bound (BLB) respectively. This is shown in

4.7 Simulation Results

It is very important to ensure that the system can self startup. In this design the worst case will be to have an empty charge pump. Still as noted, in [73] the delay cell can operate through leakage currents (although slowly). The VCO based on this cell will also startup oscillations without external influence. An example of this at light load (10uA) is shown in Figure 4.20. The negative voltage at the beginning is a result of the load being represented as a current source. The converter took about 15ms to startup. A heavier load (1mA) for the same reference (1.1V) is shown in Figure 4.21

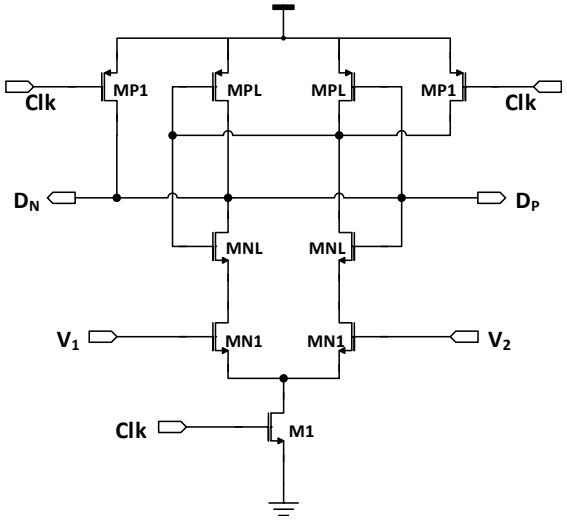
using a resistive load equivalent to 1mA.

To show that using multiple reduces ripple we have simulated the 3-phase converter and a single-phase converter with the same amount of charge transfer capacitance, at a desired reference voltage of 800mV and a load resistor equivalent to 500μA. The results are shown in Figure 4.22. The ripple value is about 50mV and 18mV in the single phase and 3-phase respectively. Note the presence of subharmonic oscillations which is a disadvantage for charge pump controllers.

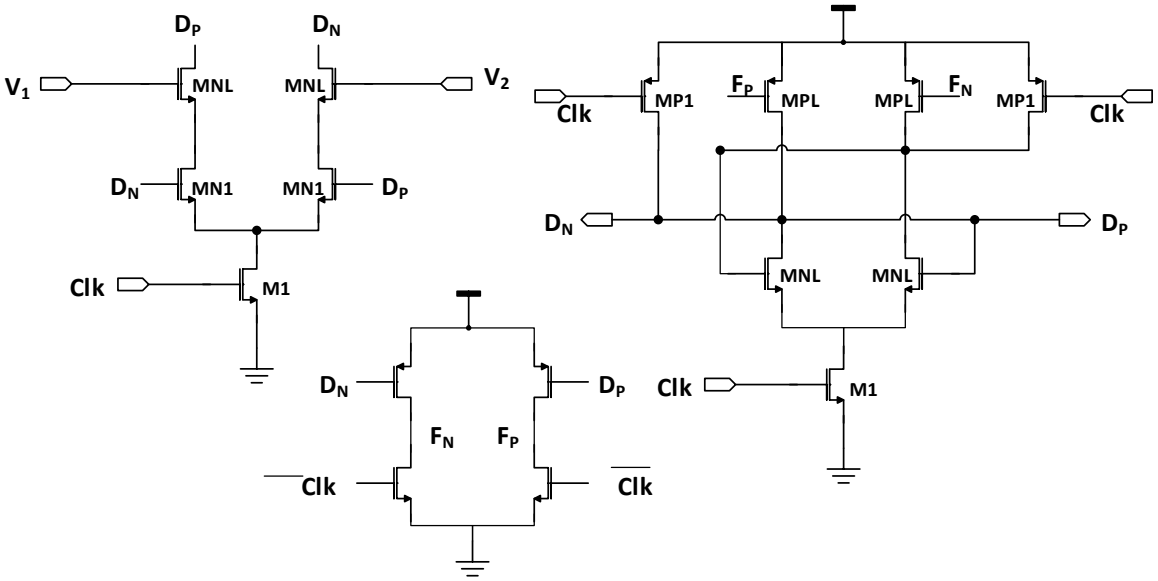
Another serious disadvantage of charge pump controllers is the very slow transient response. In Figure 4.23 the load is stepped from 100 μA to 2 mA. Although eventually the controller is able to regulate there is a large drop in the output voltage. Any load subjected to such a drop will probably shut off. A simple solution to this is to use a separate clock for the comparator This of course causes the comparator to cause losses similar to those in the Pulse skipping controller.

The efficiency as a function of the load is shown in Figure 4.24. The graph was obtained by sweeping the output load at a constant reference voltage of 800mV. The first line (crosses) shows efficiency accounting only for power stage, charge pump and VCO losses. The second line (solid circles) shows the efficiency when the decoder and driver losses are included. A reduction of about 5 % is apparent. It can be noted that this loss in efficiency is almost constant. Since the frequency is scales with the load (due to the controller + VCO), and the power stage losses also scale with the load the efficiency is expected to be almost constant.

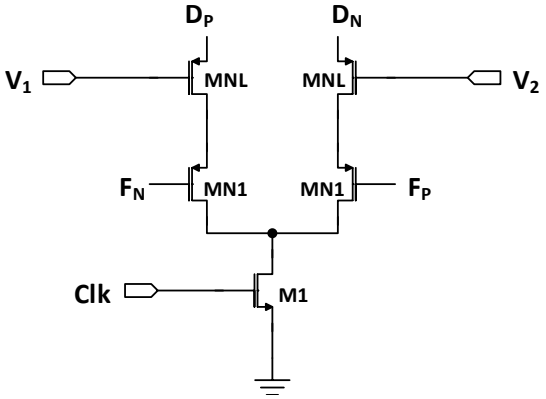
One can note that in Figure 4.24 the first points exceeds 89%, the theoretical limit of efficiency for 1/2 gain setting delivering 800mV from 1.8V supply. This can explained by looking at Figure 4.25 which shows that there is a 2 % regulation error. This means that the theoretical limit is not (800mv/900mV) but rather (820mV/900mV) = 90.6%



(a) StrongARM dynamic comparator



(b) Goll Zimmerman comparator [75, 76]



(c) Additional input stage added to Goll Zimmerman to allow rail to rail input span

Figure 4.17: Comparators

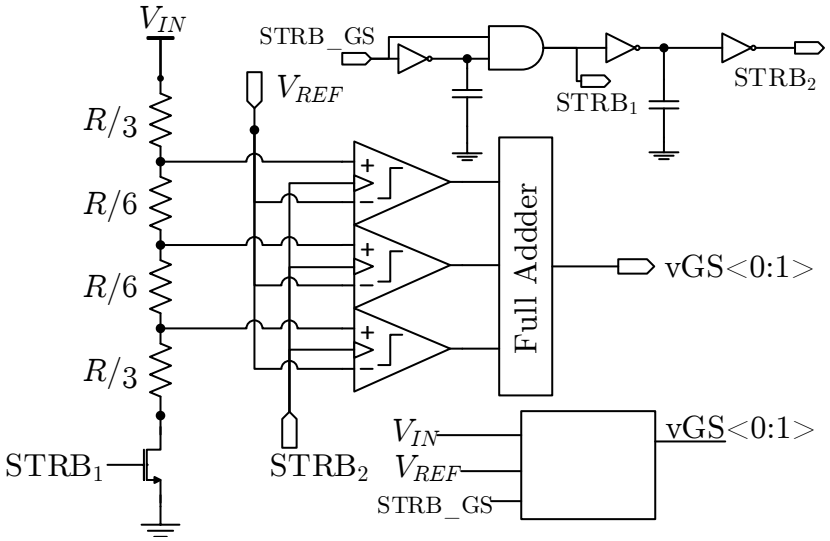


Figure 4.18: Gain settings unit: generates vGS which shows what gain setting is most appropriate

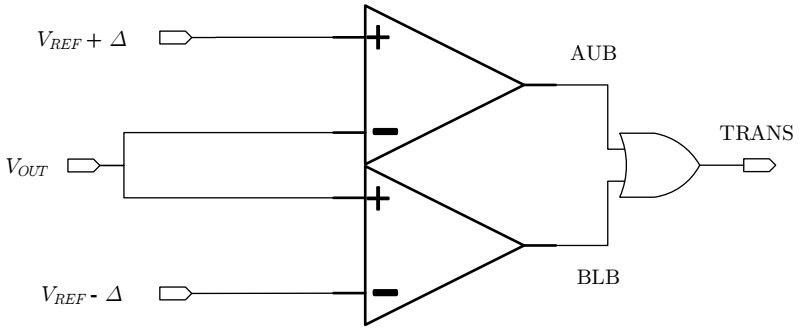


Figure 4.19: Transient detection unit

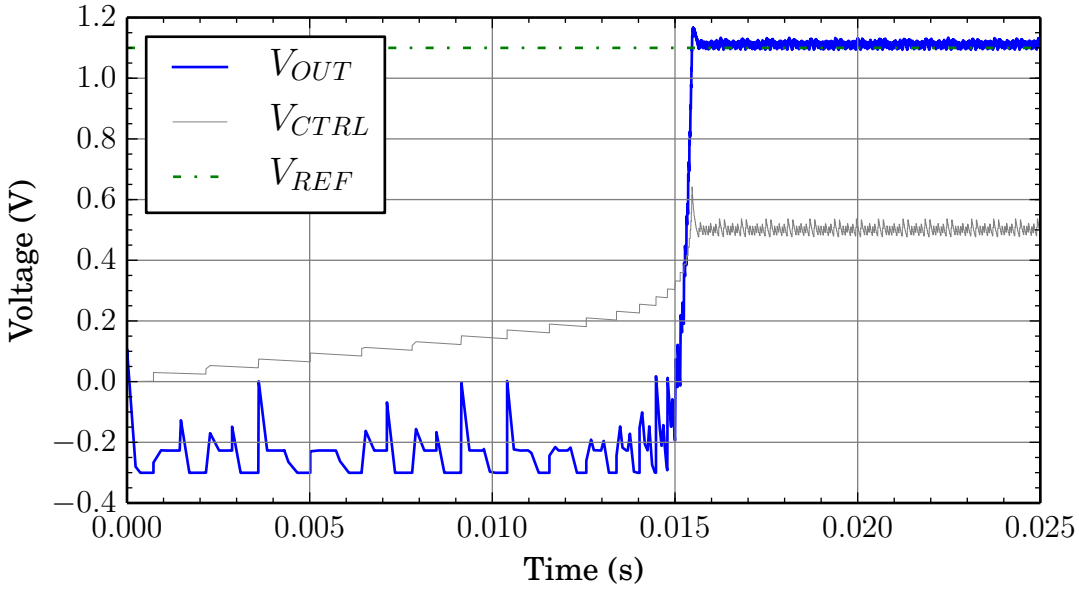


Figure 4.20: Startup with Zero Initial Voltage on Charge Pump and Output Load = 10μA.

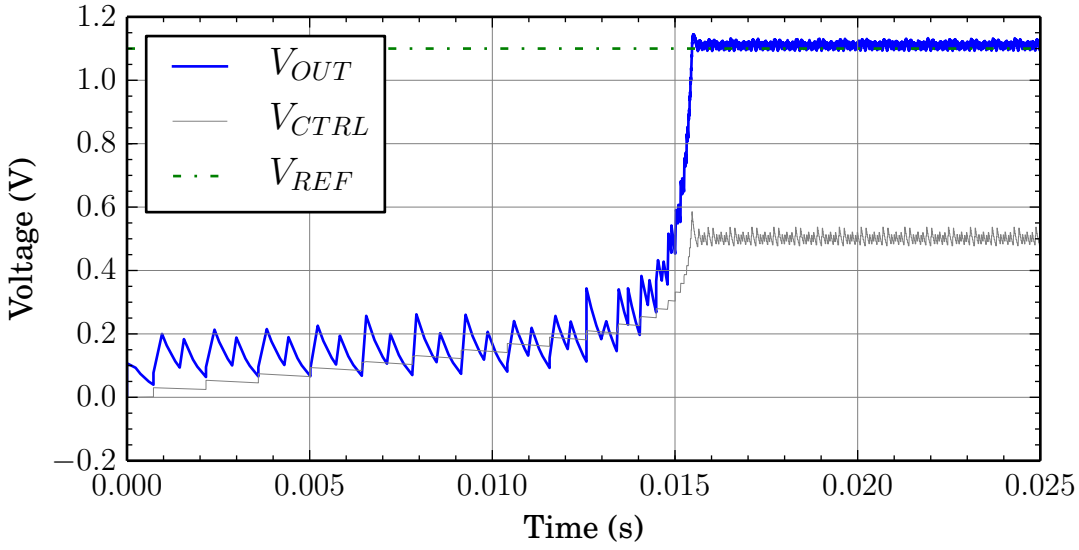


Figure 4.21: Startup with Zero Initial Voltage on Charge Pump and Output Load = 1.1KΩ

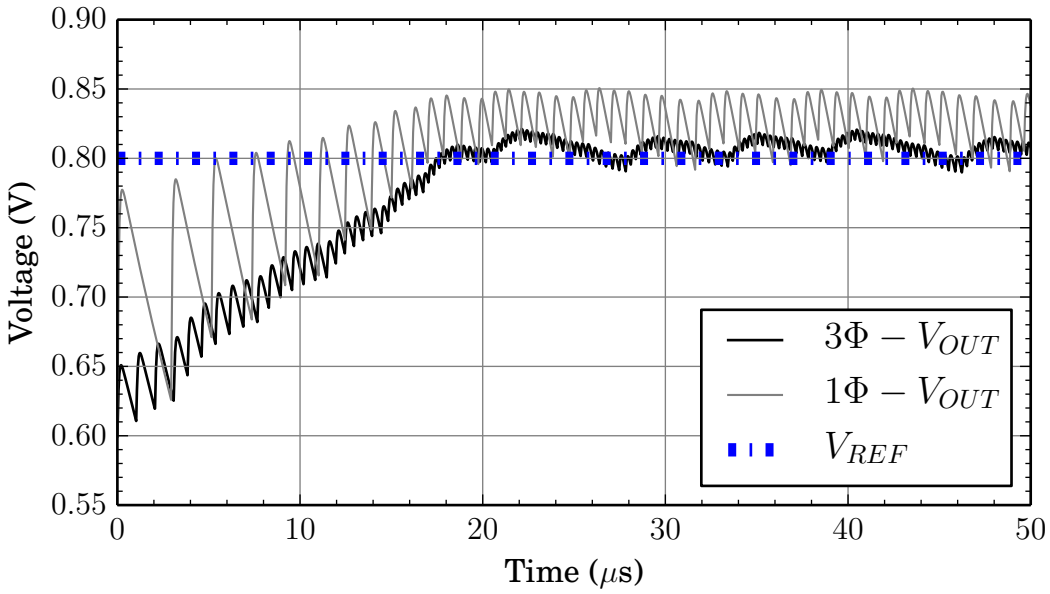


Figure 4.22: Single phase vs. Three Phase output ripple

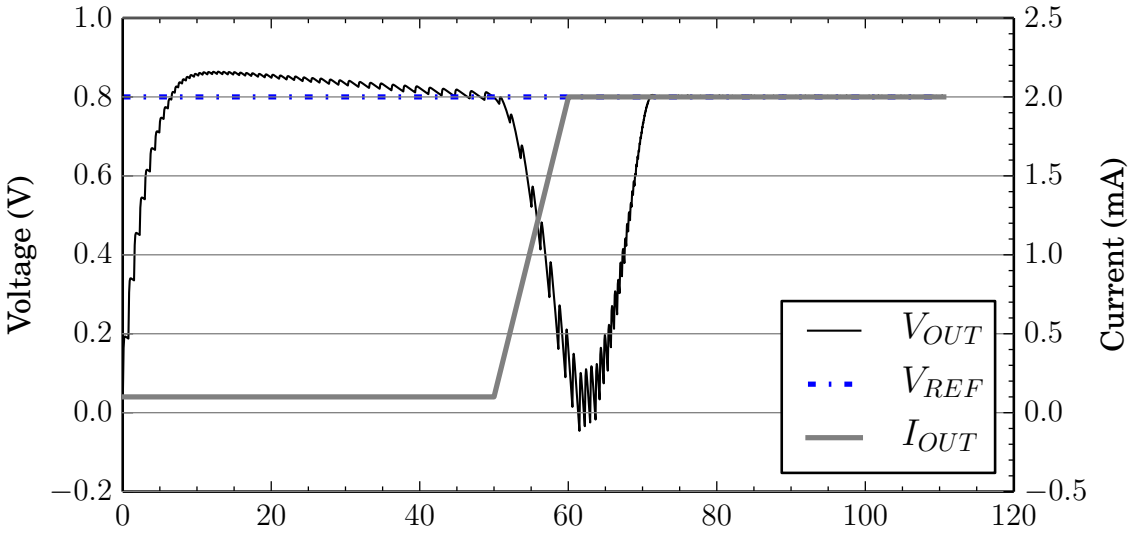


Figure 4.23: Transient performance of charge pump controlled SCC

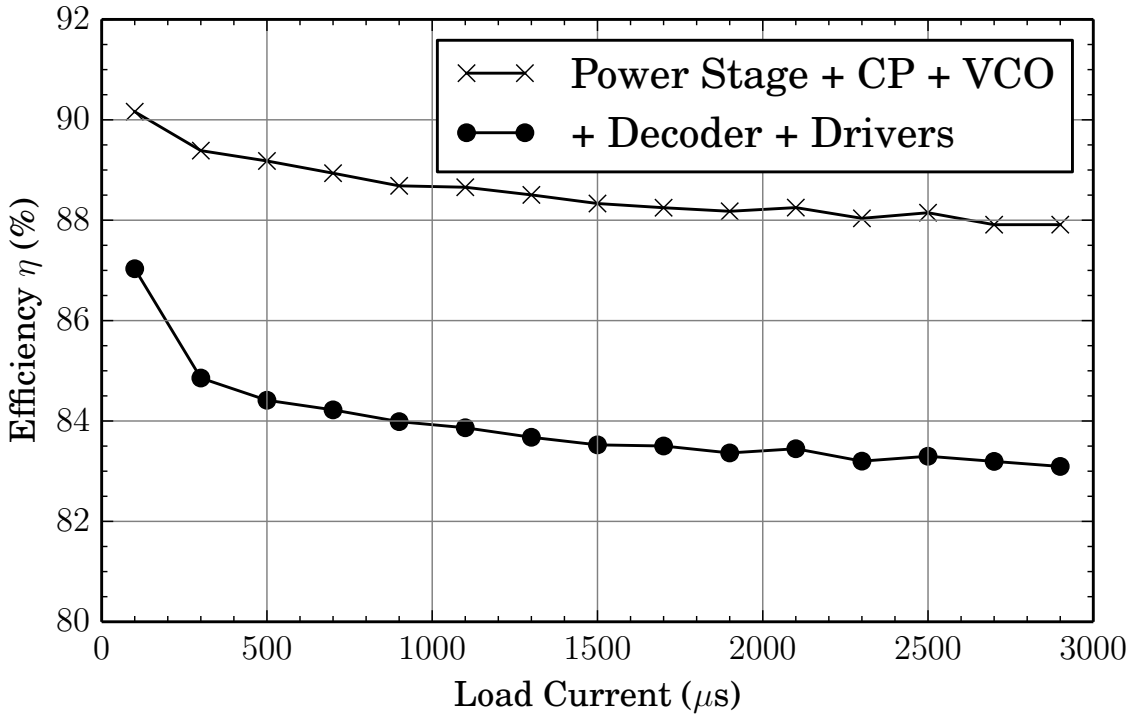


Figure 4.24: Efficiency vs. Load current for V_{REF} = 800mV

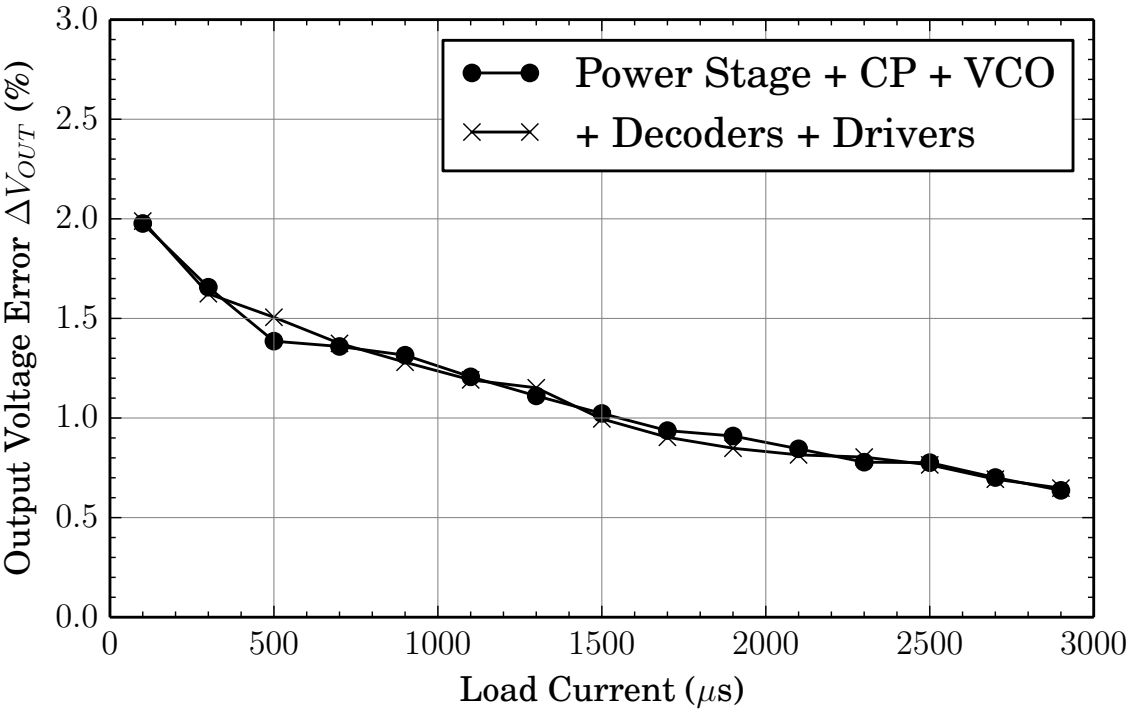


Figure 4.25: Output Voltage Error vs. Load current for V_{REF} = 800mV

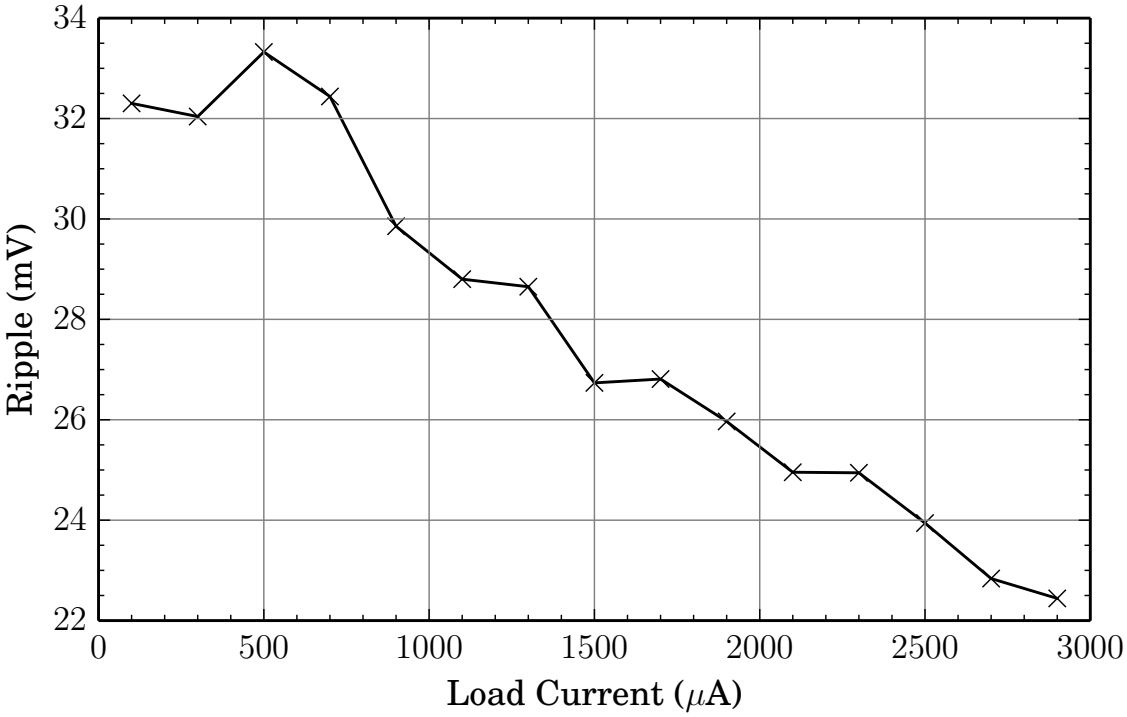


Figure 4.26: Ripple vs. Load current for V_{REF} = 800mV

CHAPTER 5

INDUCTIVE CONVERTER

In this chapter we present the design and some results of a fully integrated inductive converter. Again we follow the same procedure outlined in [BACK REF.]. We start by exploring the passive options available for implementation of the inductor and capacitor of the power stage. Since this converter shares the capacitors with switched capacitor converter the capacitors will not be discussed here.

1. Section 5.1 explores the passives available for a fully integrated converters. The two main options available in the LF150nm technology and bondwire are compared. On-Die Spiral inductors designed and extracted usig Cadence tools and CST Studio have a very high DCR that hinders efficiency of operation. Thus bondwire is the more resonable choice.

   Calculations show that the converter for most of the desired range will be operating in DCM. As such it better to use a diode to implement the low side of the switch. This allows for a simpler controller while still maintaining DCM operation.

   The sizing of the PMOS power stage switch and inverter chain driving the switch is presented.

2. Section 5.2 discusses the control circuitry used to control the power stage in 5.1. The main blocks necessary are the error amplifier, compensator and the modulators. Since this is a 4 phase converter we have multiple modulators and have to generate a 4 phase clock signals.

We present a new PWM circuit that avoids the use of comparators. For simplicity an integrator is used as a compensator.

3. Section 5.3 Some of the blocks presented in the previous section are presented as circuit level diagrams, including the edge detectors, error amplifier, and 4 phase clock generator.

4. Section 5.4 presents the results of simulating the design converter in Cadence using LF150nm technology.

5.1 Passives

The topology we have chosen is the simple buck converter. The design starts by selecting the passive components. Since the capacitor is shared with the SCC converter where we fixed it to 10nF we have only the inductor. For integrated converters the choices are either on-chip inductors or off chip but on package for example bondwires. On-chip inductors have low quality and low variability. Modeling of on-chip inductors is discussed in [53].

Bondwire inductors have better quality but suffer from high variation [12]. The placement of the die, the thickness of the bondwire material and the connection with the leads are all factors affecting bondwire value. For the purposes of this thesis we will ignore this variability.

Bondwires are complicated to model in full. However standards for simplified models exists such as [79]. Several studies also exist on detailed modeling of bondwires [80, 81]. We will use a simplified model for calculations and a 3D Field Solver (CST EM Studio) to obtain an extracted SPICE model for the bondwire.

5.1.1 Bondwire Modeling

The JEDEC5 JESD59 standard [79] specifies that bondwire loop can be approximatd as five straight segments described by five parameters. This is shown in Figure 5.1. The parameters are:

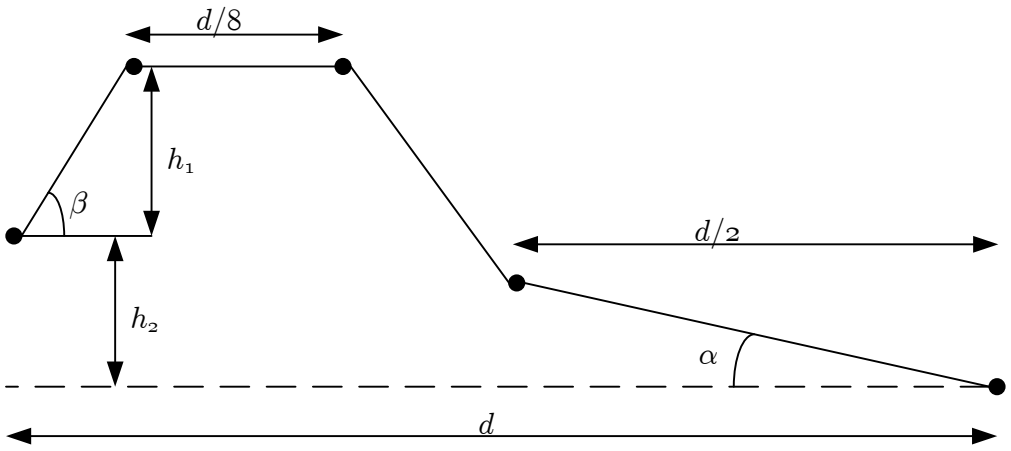


Figure 5.1: Bondwire JEDEC5 approximate model

α angle between the package lead and the bondwire.

β angle between the bondpad of the die and the bondwire

d total horizontal distance covered by the wire.

h_1 height between bondpad and the top of the bondwire.

h_2 height between the lead and the bondpad

The height of the bondpad can be approximated as the height of the die itself (725μm) [1]. The horizontal distance can be obtained from the package dimensions and the expected die dimensions. Assume a 2mm $\times$ 2mm die and a Quad Flat No-Lead (QFN) 44 pin package of dimensions 7mm $\times$ 7mm. From the package documentation the pad area is 5.4mm $\times$ 5.4mm. Assuming perfect centering of the die the horizontal distance from the leads to the die will be (5.44mm - 2mm)/2 = 1.72mm.

The angles α and β are more difficult to estimate without knowledge to estimate without knowledge of the bonding process. However approximations can be made. The JEDEC standard specifies that β can be approximated as 90°, for rough calculations. With β collapsed to 90, α can be estimated.

After these paramters are estimated, the length of the bondwire can be calculated. From this first order approximations can be obtained for the resistance and inductance.

[1] LFoundry uses 200mm wafers. Wafer sizes are standardized with 200mm wafers having a 725μm thickness

The length turns out to be about 2mm. Several standard bondwire diameters are used. For copper one of the standards is 25μm [2].

Using the formulae from the JEDEC standard formula for inductance [79]:

$$L = 2l\left[\ln\left(2\times\frac{l}{r}\right) - 0.75\right]\text{nH} \tag{5.1}$$

Where l and r are the length and radius of the bondwire. Performing this computation we obtain a value of 2.034nH $\approx$ 2nH. This is close to the approximate value of 1nH/mm in [17]. The resistance can be computed as [79]:

$$R = \rho\frac{l}{A} = \rho\frac{l}{\pi r^2} \tag{5.2}$$

using $\rho = 1.68\times10^{-8}\Omega/m$ we perform this computatio. The resistance value is 70mΩ. This is about half compared to 55mΩ/nH, the value in [17]. The difference is probably due to difference in material (aluminum vs. copper).

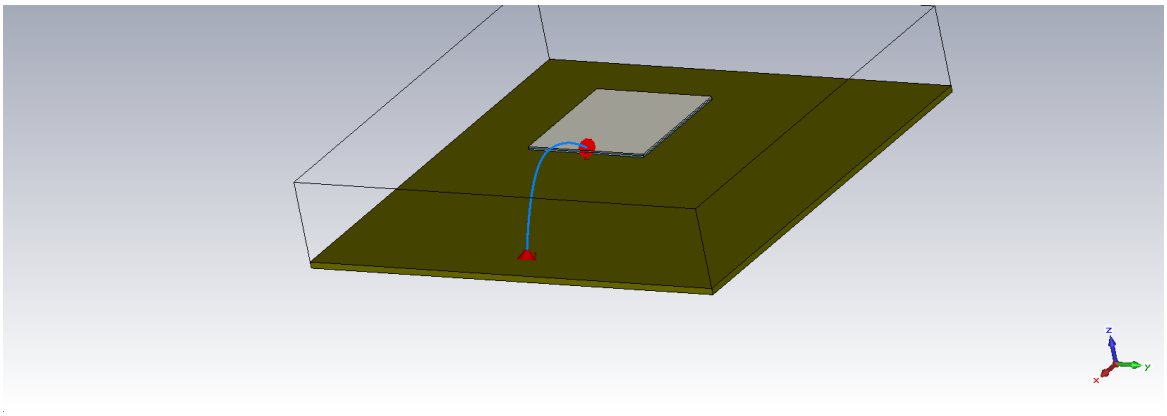
Using CST EM Studio we modeled bondwire with the same assumptions as before but with spline (curved shape) instead of the approximate JEDEC5 model. The results model and netlist are shown in Figure 5.2.

5.1.2 Modelling of On-Chip Spirals

The LF150nm technology has 7 metal layers available METAL1 METAL2, through to METAL5, METALF and METALT. The last METALT is a thick metal ($6\mu m$) layer. We designed sqaure spirals with an area of $800\mu m\times800\mu m$. Maximum track widths of $40\mu m$ where used to reduce the resistance. Then the parasitic extraction tool (Assura and Quantus Extraction) was used to extract the parasitics. The AC response of this circuit was determined and used to calculate the equivalent DCR and inductance.

Three inductors were modeled: a single METALF spiral, a multi layer formed from METAL2, METAL3 ... up to METALF and finally a METALT spiral. We note here

[2]The LF150nm process has 80μm pads. Bondwire should have sufficient margin. Amongst the standard sizes 25, 75 and 250m, 25μ makes the most sense



(a) Model used in CST EM Studio for extracting bondwire equivalent circuit

```
*****************************************************
*  SPICE Netlist generated by CST MICROWAVE STUDIO.


*****************************************************
*  Interface (wire specification)
*****************************************************
*  Wire 1: Port (Mode) A: 1 (1) / Port (Mode) B: 101 (1)
*  Wire 1:  Inner Node A: 11    /  Inner Node B: 12
*****************************************************
.subckt SCirTL
+ 11 12
*****************************************************


R1      11 20 2.36429
R2      22 23 2.36429
L1      20 21 8.84413e 010
L2      21 22 8.84413e 010
C1       21 0 1.07277e 013
R3       21 0 4324.61
R4      23 24 2.36429
R5      26 27 2.36429
L3      24 25 8.84413e 010
L4      25 26 8.84413e 010
C2       25 0 1.07277e 013
R6       25 0 4324.61
R7      27 28 2.36429
R8      30 12 2.36429
L5      28 29 8.84413e 010
L6      29 30 8.84413e 010
C3       29 0 1.07277e 013
R9       29 0 4324.61

*****************************************************
.ends
```

(b) Model used in CST EM Studio for extracting bondwire equivalent model

Figure 5.2: 3D model is CST EM Studio and extracted Netlist

that the extraction for METALT layer does not allow for inductance extraction. We used CST Studio to model the METALT inductor. The results of this exercise and the

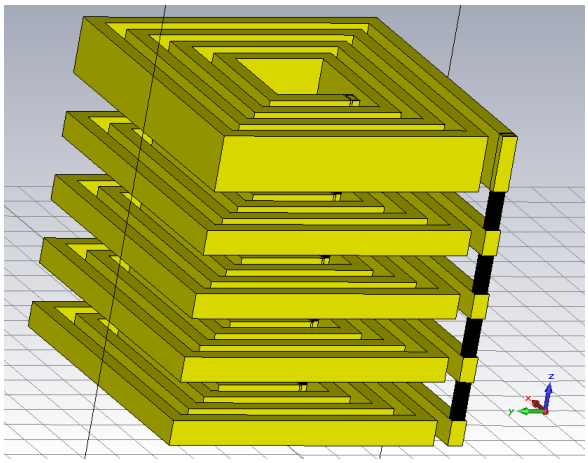


Figure 5.3: Multi Layer Spiral model in CST Studio. Z-axes scaled around 300 times.

Table 5.1: Comparison of Inductors Available for Fully integrated converters

Inductor Type	On-Chip Size	L (nH)	DCR Ω	Notes
Single Layer Spiral using METALF	$800\mu m \times 800\mu m$	11.5	9.54	Space under inductor availabel for use.
Multi Layer Spiral using METAL2,3,4,5 and METALF	$800\mu m \times 800\mu m$	10	3.54	Very limited use of space under inductor
Thick Metal Layer (METALT) (CST-Studio)	$800\mu m \times 800\mu m$	6.828	0.63	Space under inductor available. LF150nm has no extraction for METALT
Bondwire	2 pads $80 \times 80\mu m^2$ each.	2	0.07	High variability

modeling of bondwire are shown in 5.1. As can be seen clearly bondwires offer the best DCR per inductance ratio and hence can be expected to produce better performance. Thus we will choose bondwires for our converter.

5.2 DCM Operation

Figure 5.4 shows the inductor current for a power stage containing an NMOS switch and PMOS switch at a load of 18Ω. This shows the main issue with operating in CCM

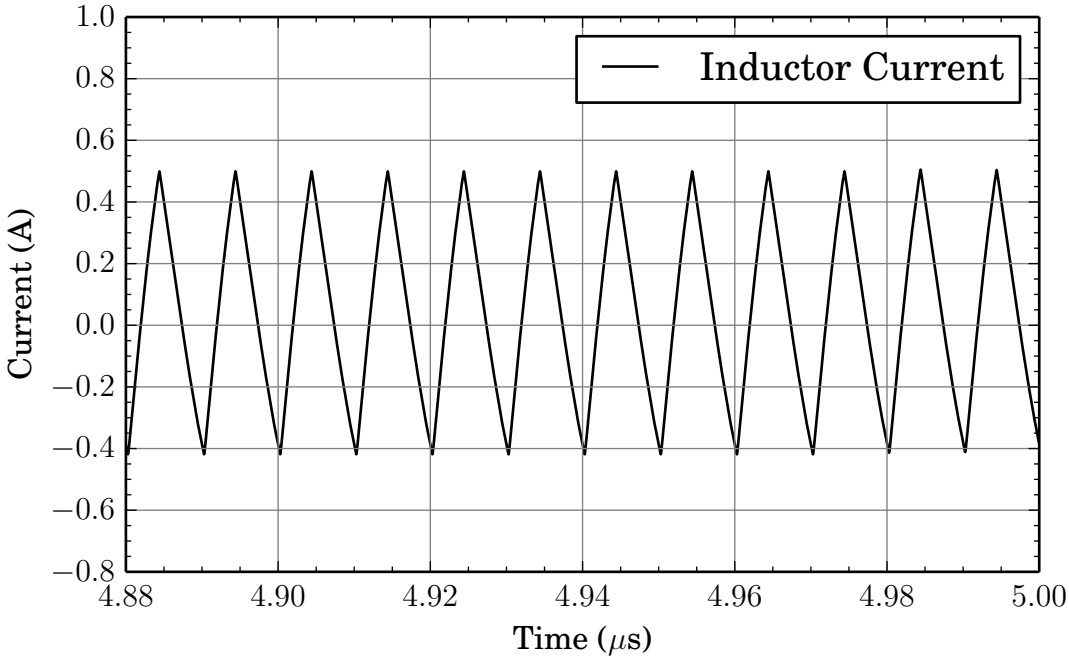


Figure 5.4: Inductive Converter CCM Mode inductor current at load of 18Ω

using small inductor values. The inductor current ripple is larger than the average load current it self. As such there are points in time where the inductor current goes negative. In CCM this will be through the NMOS switch. This reverse current discharges the output into ground, harming both efficiency and regulation.

The solution to this as explained in [17] is to operate in DCM. DCM however is difficult to achieve at high frequencies because of the small delays available. In [17] the authors propose calibration loops to obtain precise DCM operation. However the circuits used are relatively complex. A simpler method is to use a diode in place of the NMOS switch. the downside of this is a possible reduction of efficiency if the inductor is strong enough to cause a "kick-back" current through the diode.

For a Buck converter using an inductor L and ignoring all parasitics, the current below which the inductor current goes negative (and hence operating in DCM becomes recommended) is given by [9]:

$$I_{Load} \leq \frac{(V_{in} - V_{out})(V_{out}/V_{in})T}{2L} \tag{5.3}$$

A quick calculation given the values of inductance from the bondwire shows that even at currents of 1A and an output voltage of 1.35V (conversion ratio of 0.75) that the converter is still operating in DCM. This justifies our use of the diode. For typical converters at high load currents and CCM operation the NMOS switch is better since it does has a lower drop (and losses than the diode). In this design there is no CCM even at high loads because of the low inductance provided by the bondwire.

5.3 Overall Converter and Controller Design

The overall diagram of the converter is shown in Figure 5.5. The power stage shows the diode now replacing the NMOS switch. The output voltage is comapred to the reference voltage V_{REF} by an Error Amplifier Compensator block. The output of the error amplifier and compensator block goes to the PWM modulator which generates a PWM signal. The driving capability is boosted by the drivers and finally applied to the PMOS switch S_P. The individual circuit blocks are described later.

Note that different from typical designs we are using one opamp as an error amplifier and compensator at the same time. This slightly reduces the control overhead. Further note that different from traditional designs which employ an off-chip potential divider at the output to bring the output voltage in the common mode range of the error amplifier we chosen *to boost the supply of the error amplifier*. The use of off chip resistors is favored usually because: an accurate division ratio requires precision resistors and low power consumption requires large resistors. Large precise resistors are usually not found in current integrated circuit technologies. The voltage is boosted by means of a Favrat doubler cell [82].

The compensator circuit is shown in Figure 5.6. The circuit overall (including the internal pole of the opmp) provide the characteristics requires to stabilize the circuit. However in simple terms we can “partition" the operation as follows: the first pair R_1, C_1 shunt out the high signal ripple before it reaches the amplifier. At low frequencies the combination of R_1, R_2, C_2 form an integrator that provides the high DC gain required to reduce steady state error.

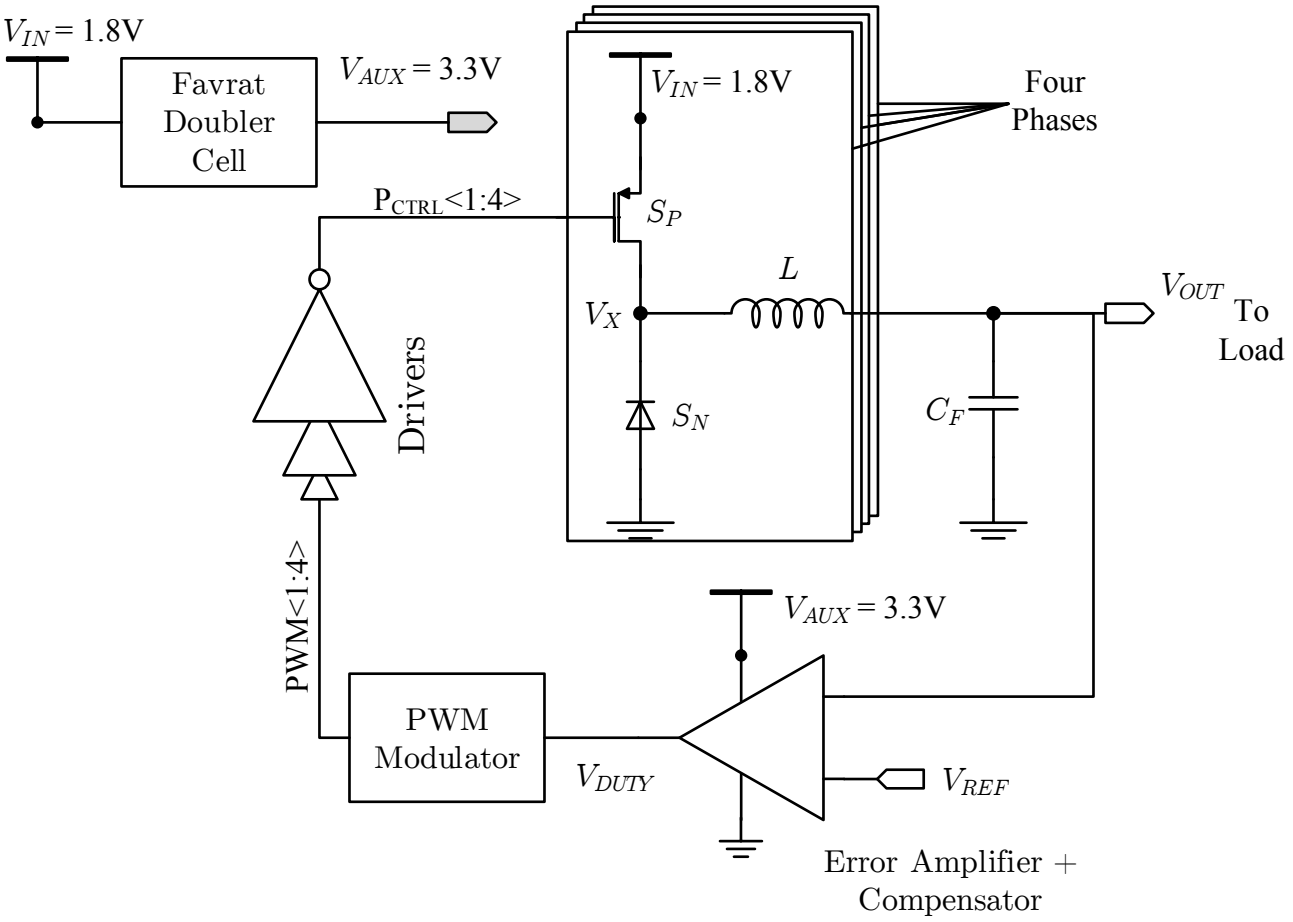


Figure 5.5: Overall diagram of inductive converter

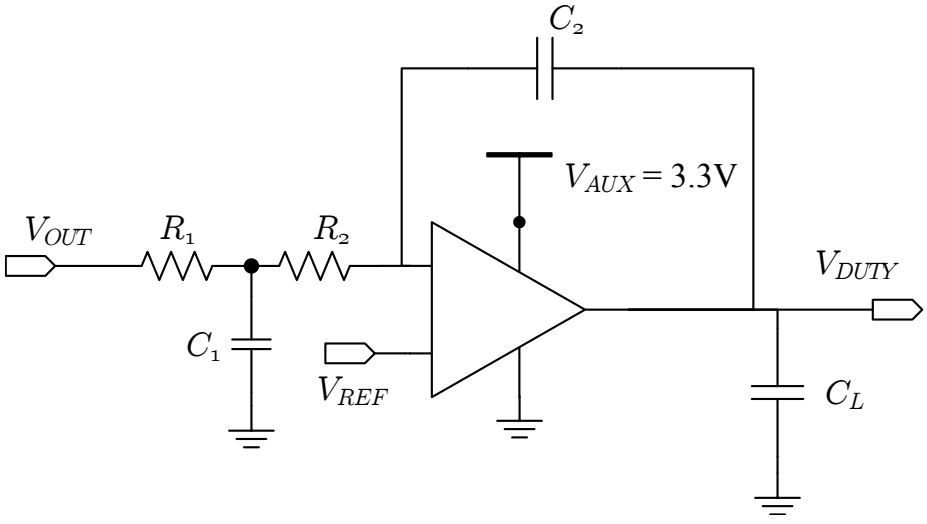


Figure 5.6: Compensator + Error Amplifier Circuit

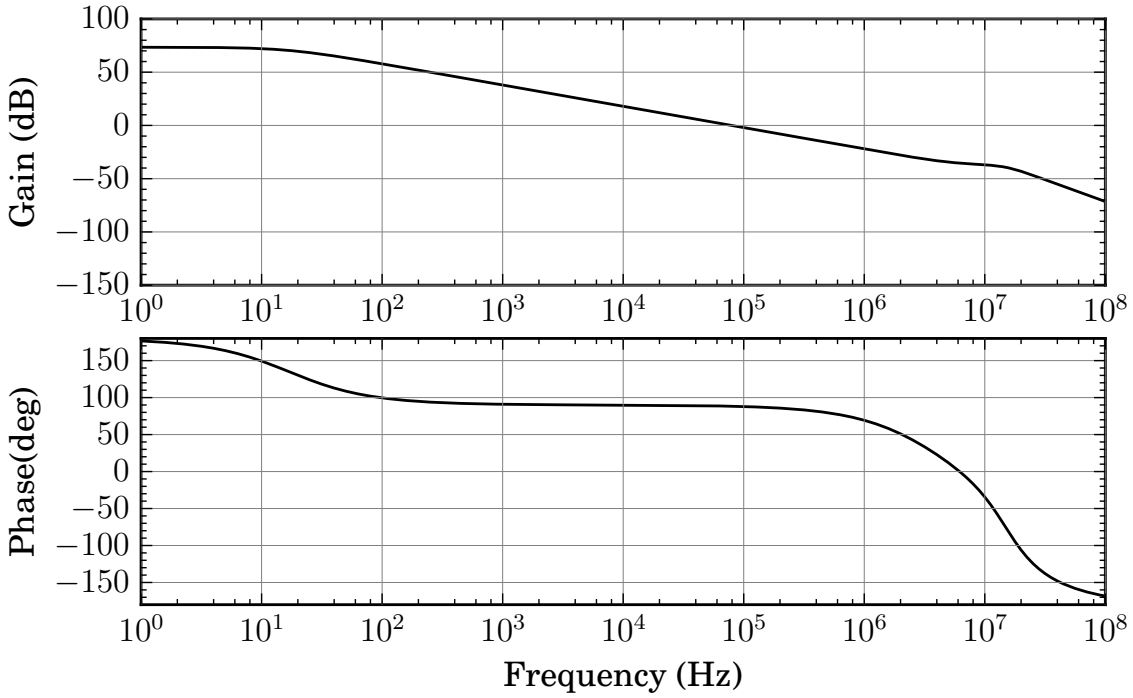


Figure 5.7: Frequency Response of the Compensator + Error Amplifier

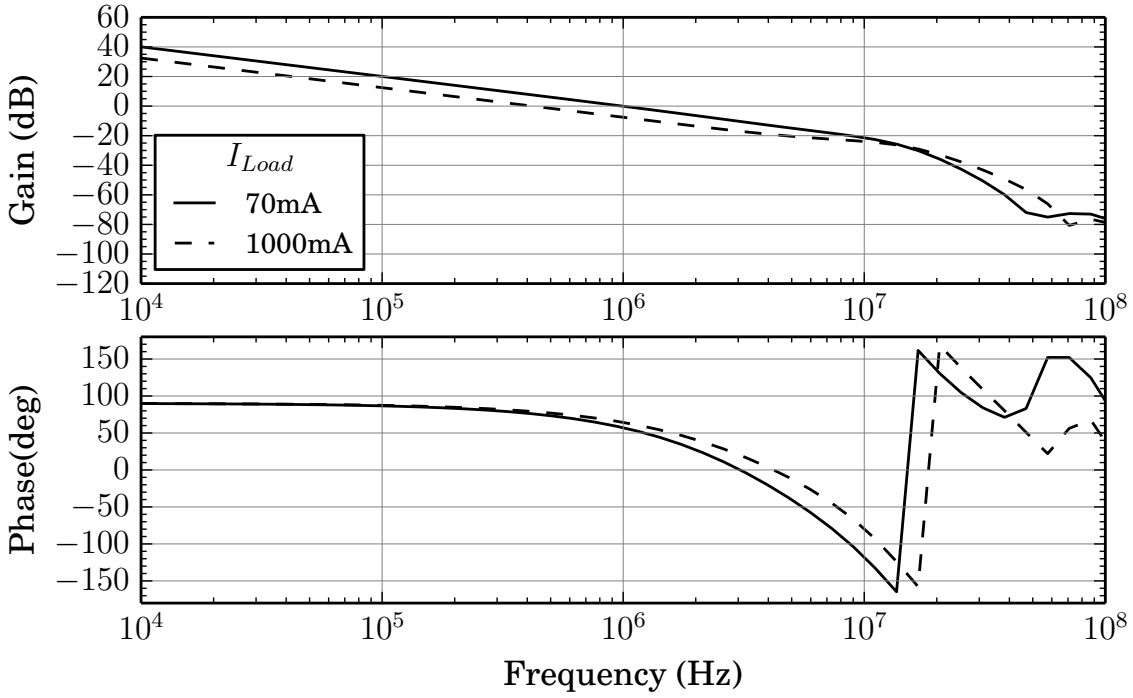


Figure 5.8: Overall converter loop response at heavy load (1000mA) and light load)(70mA).

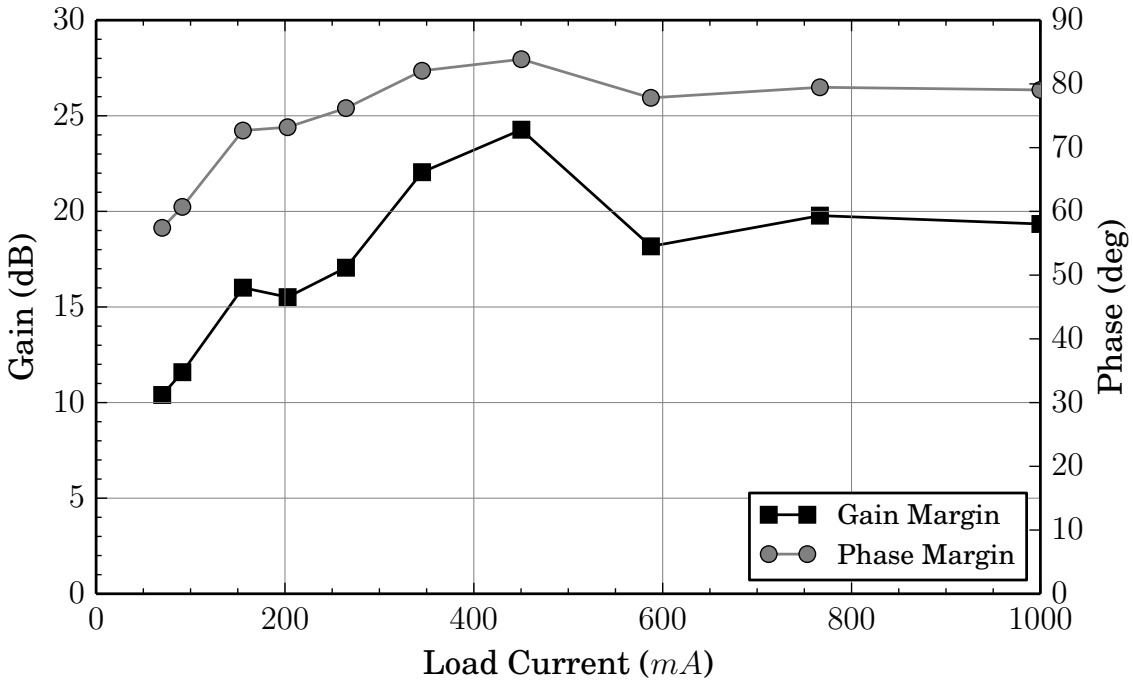


Figure 5.9: Phase and Gain margin of Converter as a function of load current.

Note that load capacitor in the compensator is placed to further "clean" and shunt out any remaining ripple. The compensator output is shown in Figure 5.7. The loop response of the overall stable converter is shown in figure 5.8 for heavy load (1000mA) and relatively light load (70mA) at $V_{REF} = V_{out} = 1.0$. The phase margin and gain margin of the converter are shown in figure 5.9. These show that as the load decreases the phase margin decreases but remains in the bounds required for stability.

5.4 Circuit Blocks

5.4.1 Operational Amplifier

The operational amplifier we chose to use is a two stage operational amplifier due to the high gain it can provide. The biasing is provided by folded cascode mirrors. To allow the common mode range to span the whole desired output voltage range of the converter and reduce design constraints imposed by the low supply voltage, we decided to use a higher supply. this is provided by an on-chip voltage doubler discussed in the

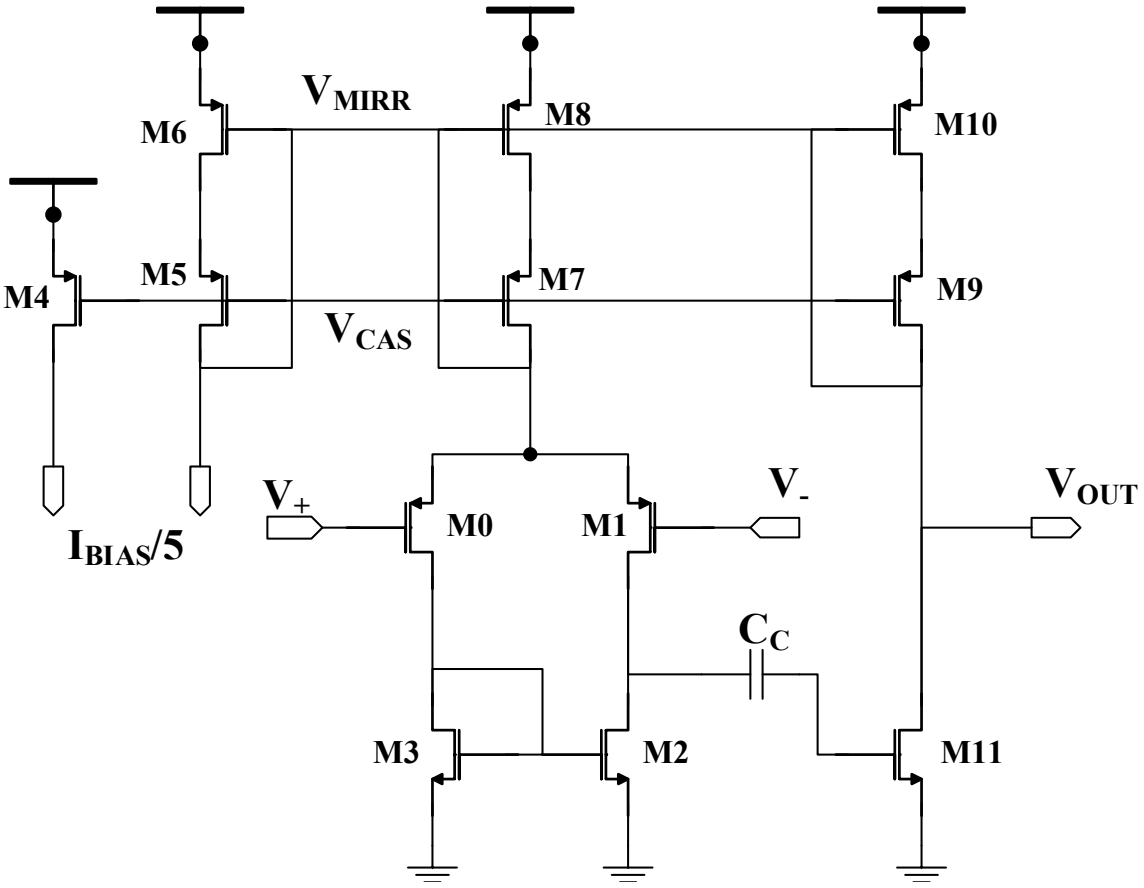


Figure 5.10: Two Stage Operational amplifier circuit.

section 5.4.3. The performance parameters of the opamp are as follows:

- DC Gain = 73dB
- Slew Rate = 1.74V/us
- Unity Bandwidth = 10MHz
- Current Consumption = 100μA — 200μA.
- Phase Margin = 50

5.4.2 Edge Detectors

The edge detector consists of a capacitor loaded inverter followed a NAND gate or NOR gates depending on the edge to be detected: NAND for rising edge and NOR

for falling edge. Figure 5.11

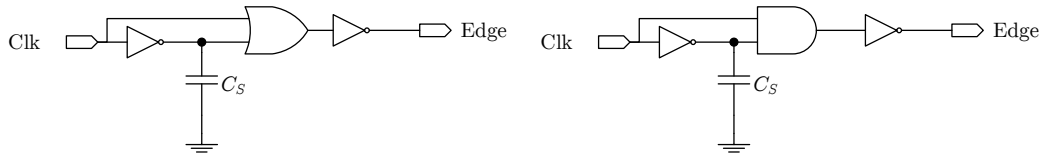


Figure 5.11: Edge Detectors for falling and rising edges proposed in [16, 17]

5.4.3 Voltage Doubler

The voltage doubler provides an output of 3.3V given an input of 1.8V. The details of the operation and performance analysis can be found in [82]. The circuit is based on the Nakagome charge pump [83], where NMOS are used as high side switches. The circuit is shown in Figure 5.12

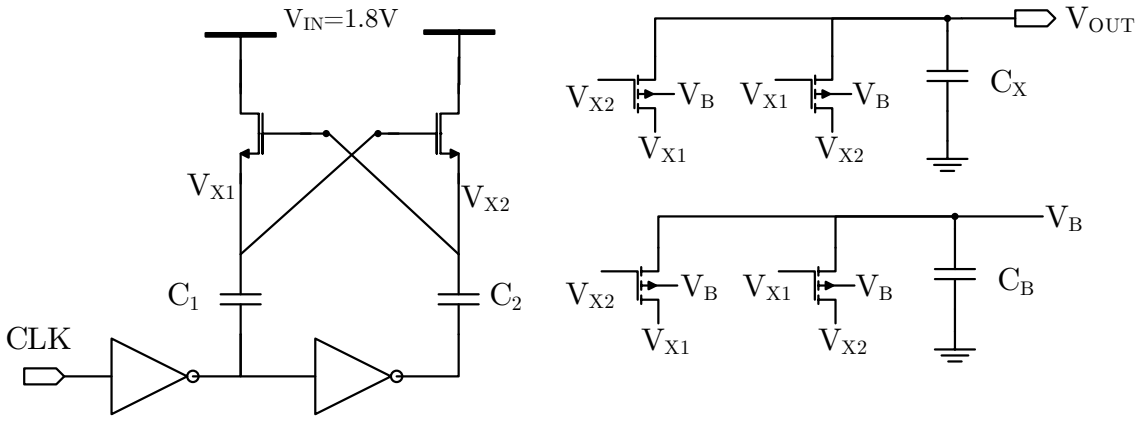


Figure 5.12: Favrat doubler cell. Cross coupled NMOS and capacitors are Nakagome Charge pump.

The load of the doubler is known ahead of time (opamp with a loading of 200μA). To reduce overhead we will use the doubler unregulated. This can be further justified by noting the desired voltage, 3.3V, is very close to the no load value of the doubler (3.55V) hence the need for regulation is reduced. We simply have to slightly over-design the driving frequency and load current to ensure proper operation at all times. The startup transient of the doubler is shown in Figure 5.13.

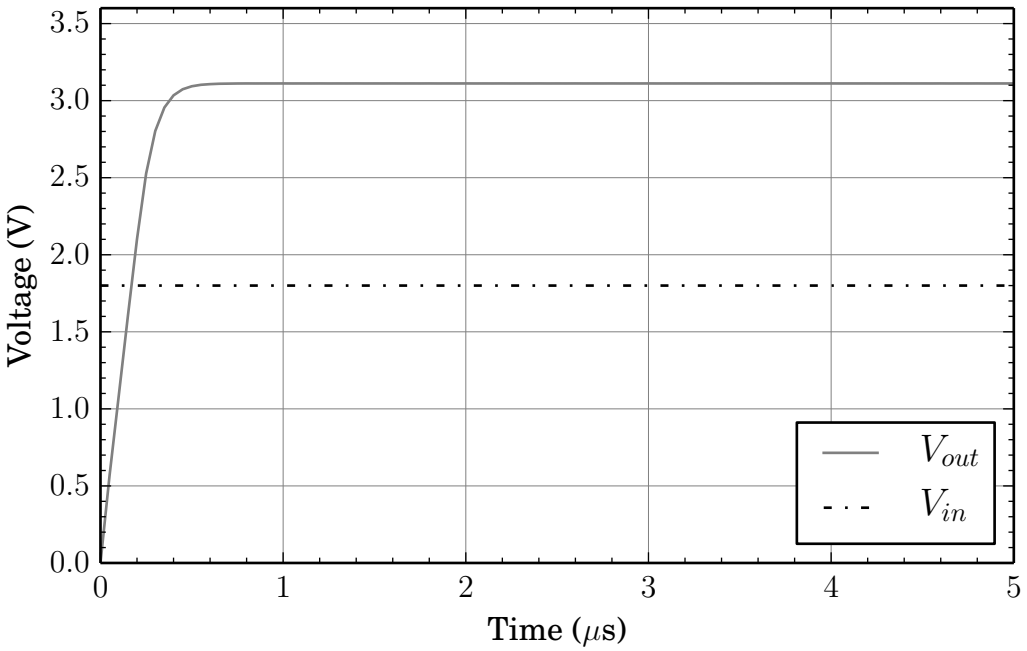


Figure 5.13: Startup Transient of Favrat Doubler Cell at clocking frequency of 100MHz and loading of 200μA

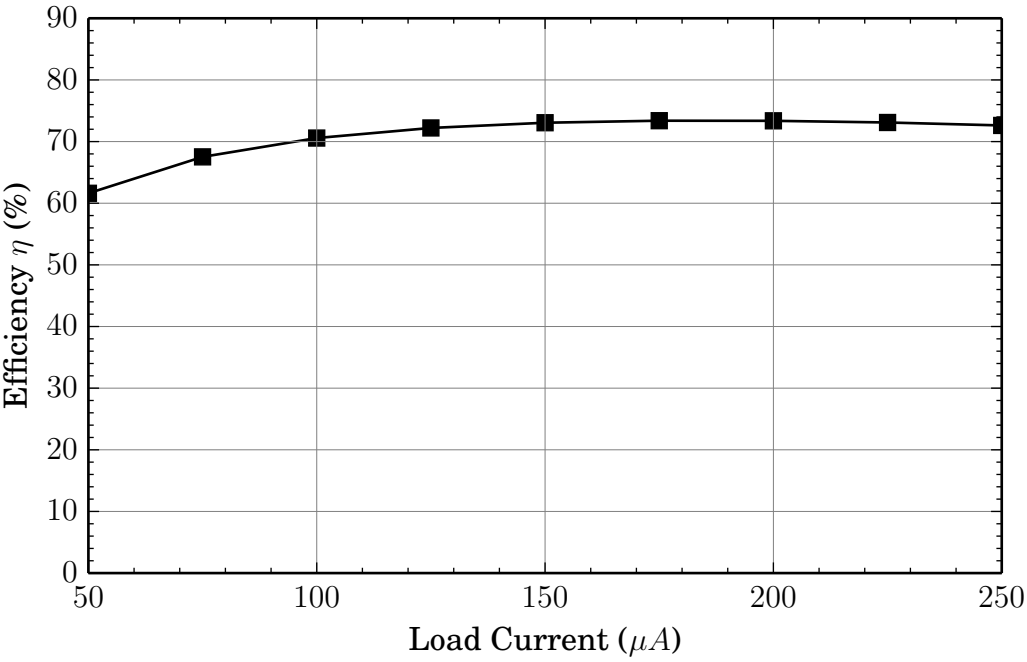


Figure 5.14: Efficiency of Favrat Doubler Cell as a function of Load Current

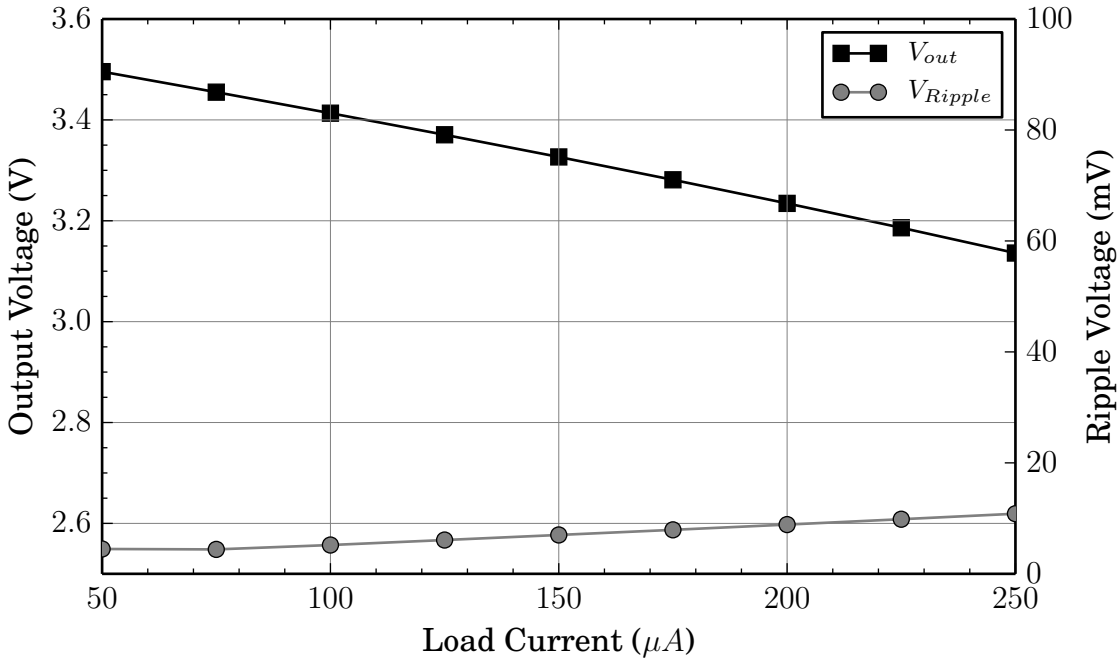
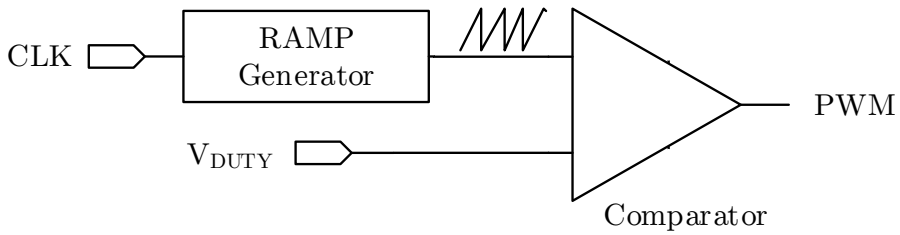


Figure 5.15: Output voltage and Ripple of Favrat Cell as function of Ripple

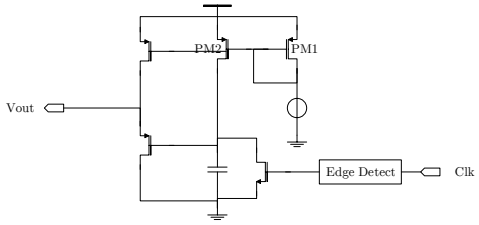
5.4.4 PWM Circuit

The PWM circuit is a typical RAMP and comparator based PWM Circuit as shown in Figure 5.16. The ramp generator consists of an edge detector and current mirrors to charge a capacitor. Every rising edge of the clock (cycle start) the capacitor is cleared to zero. The current then charges the capacitor up. To be able to use this ramp for the self biased comparators the signal must be at all times higher than the threshold of the MOSFETs. This achived by level shifting the RAMP through a source follower circuit.

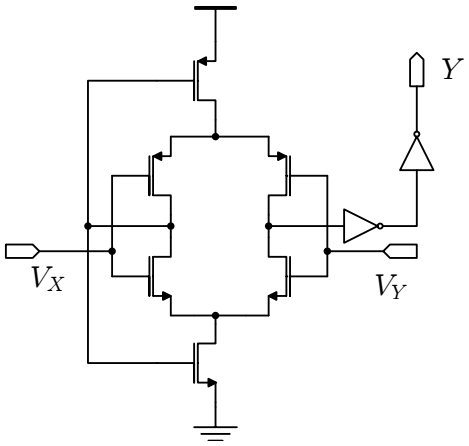
The comparators used unlike for SCC converter need to be asynchronous. An example of an asynchronous comparator with little static power consumption is the self biased comaparator [84]. Note that due to the use of both NMOS and PMOS input transistors, the input range is limited from both sides. A supply of 1.8V with thresholds of 0.4 V and 0.5 V for the NMOS and PMOS gives a range from (0.4 - 1.4 V) which fits our purposes.



(a) PWM Circuit



(b) Ramp generator



(c) Self Biased Comparator

Figure 5.16: PWM Circuit and its subcircuits

5.5 Simulation Results

In this section we present some simulation results of the inductive converter designed in this chapter. We start by showing that the system can regulate itself at startup. Figures 5.17 and 5.18 show the the startup transient for a loads of 10mA and 1A respectively. The data shown is interpolated at $5ns$. The system is able to regulate starting from 0V output to any of the desired voltages in about $5\mu s$.

The falling and rising load transients are shown in Figures 5.19 and 5.20. The converter is able o regulate after $3\mu s$. However, voltage droop is considerable. This can be reduced by either increasing the frequency (more losses) or reducing the phase margin of the compensator/error amplifier (which jeopardizes the stability of the converter.)

The falling and rising reference transoents are shown in Figures 5.21 and 5.22. The results show that the converter can well track the reference transients. The converter quickly ($< 2\mu$s) recovers the desired reference voltage. On the rising side the voltage is regulated very well and only experiences small jumps. The voltage droop when the output voltage is falling is however relatively large. This can shut off the connected load if it depends on some minimum voltage.

Figure 5.23 shows the efficiency as a function of output load current. The efficiency is shown for various load currents and output voltages. The efficiency is always higher than that of an ideal LDO. Figure 5.24 shows the difference between our converter and an ideal LDO for output voltages 1.35V and 0.9V. These correspond to conversion ratio of 75% and 50% and ideal LDO efficiencies of the same numbers. An efficiency improvement of 7% and 15% can be seen compared to the ideal LDO at 1.35V and 0.9V respectively. Note that the efficiency is low at lower output voltages. This is a direct consequence of the low inductance of the bondwires models used.

The ripple as a function of load current is shown in Figure 5.25 for various output voltages. The ripple is aways below 30mV and decreases with output voltage.

Finally,

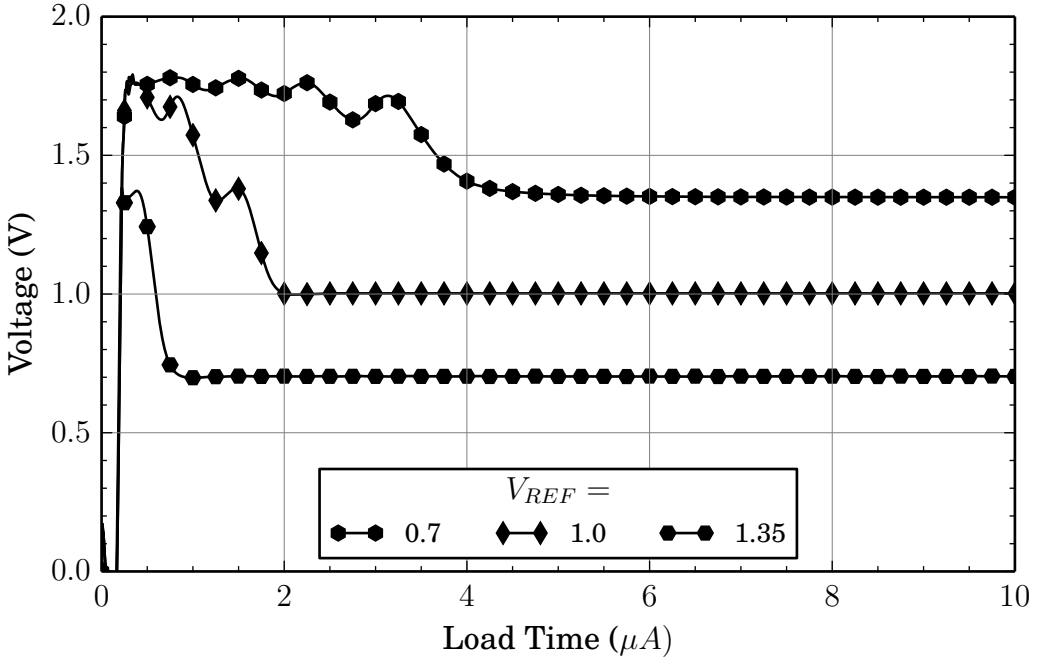


Figure 5.17: Startup Transient for $I_{Load} = 70mA$. Data downsampled at $5ns$

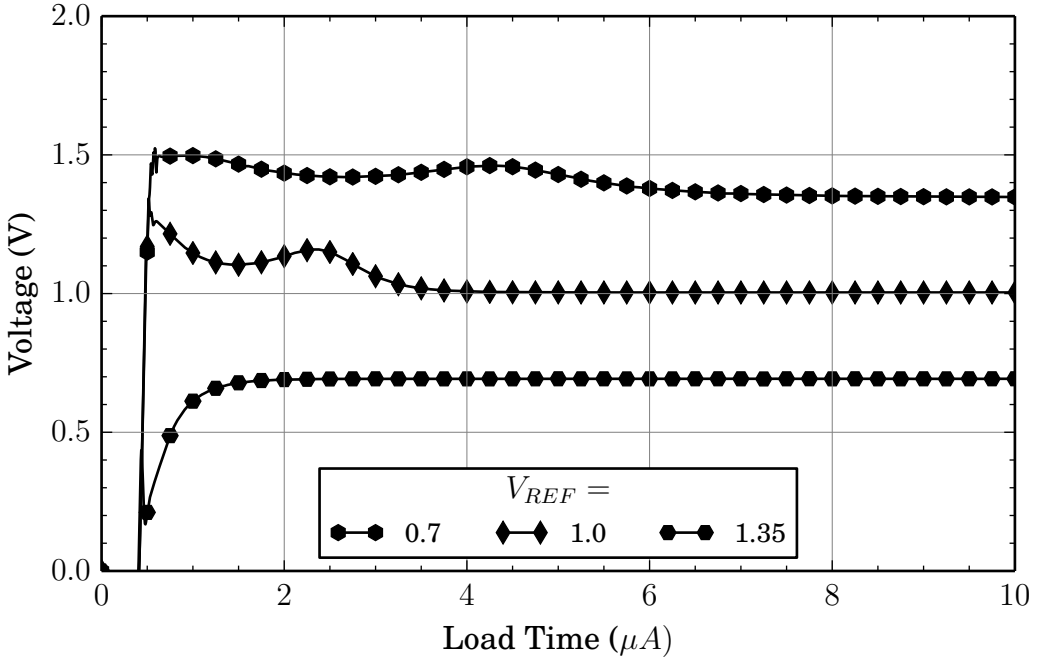


Figure 5.18: Startup Transient for $I_{Load} = 1A$. Data downsampled at $5ns$

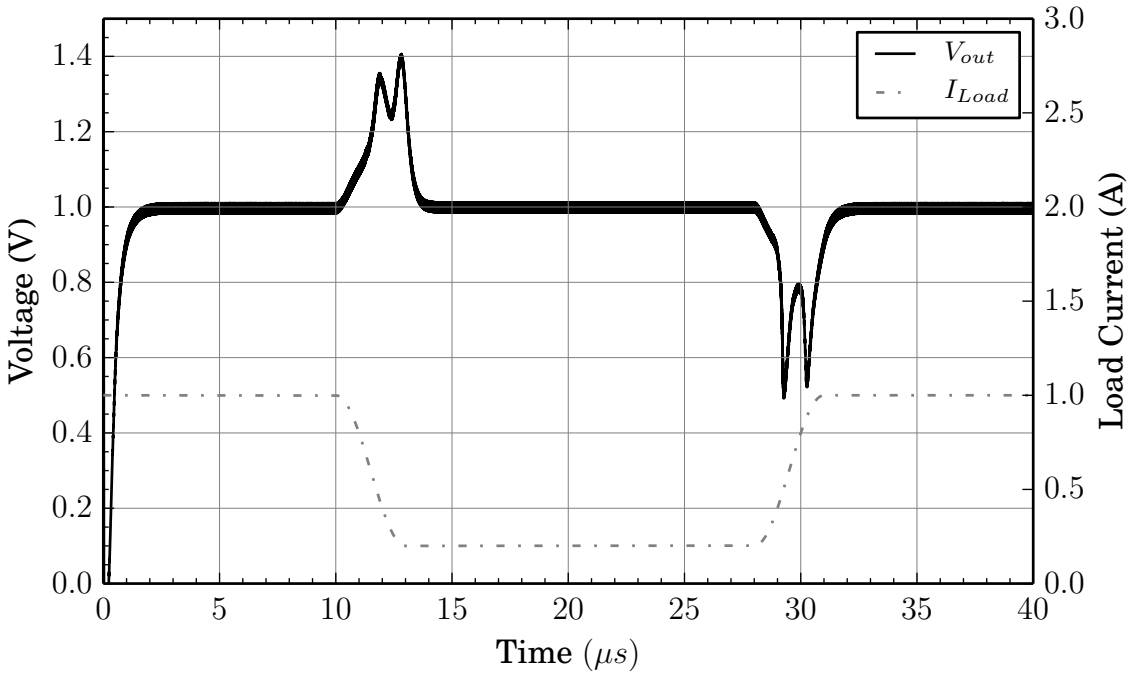


Figure 5.19: Falling pulse Load Transient. From 1A to 200mA Rise and Fall times of $3\mu s$

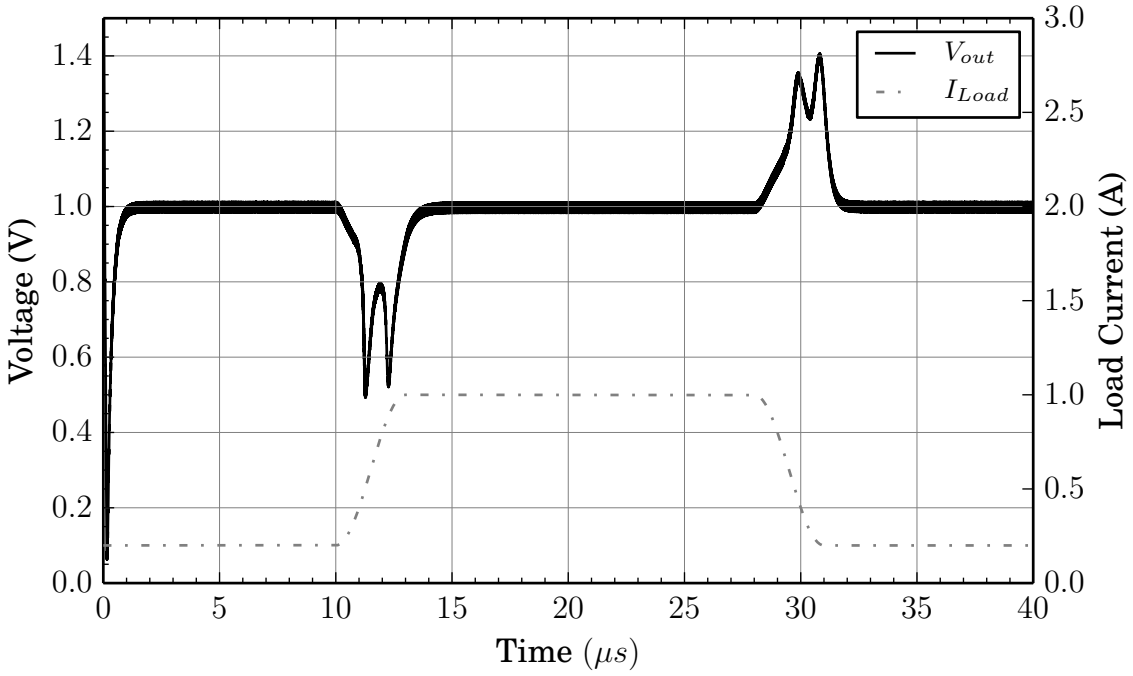


Figure 5.20: Rising pulse Load Transient. From 200mA to 1A Rise and Fall times of $3\mu s$

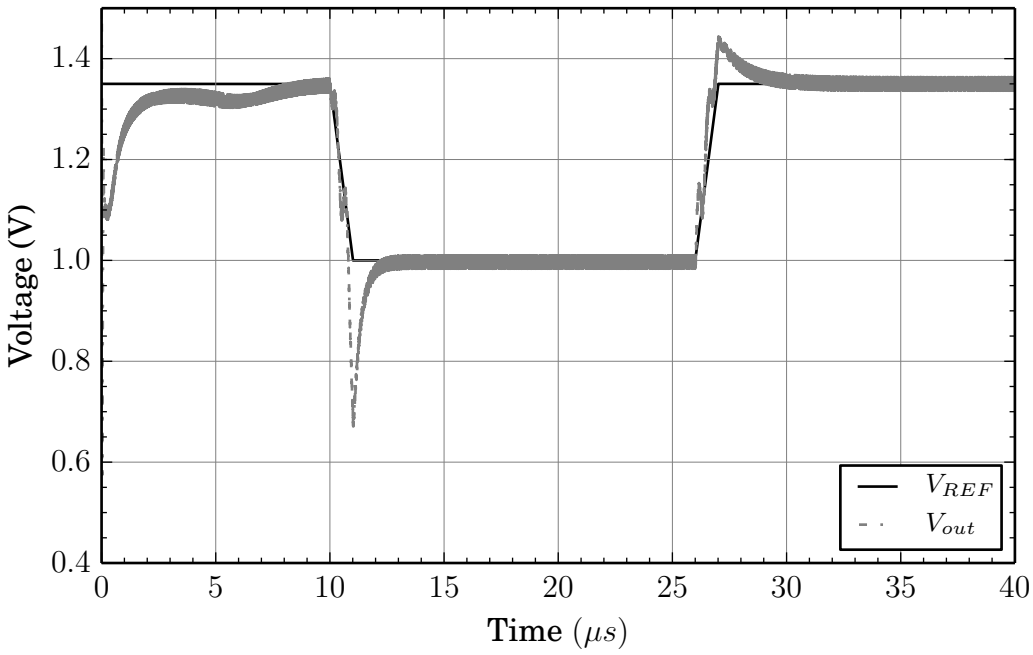


Figure 5.21: Falling pulse reference Transient. From 1.35V to 1.0V. Load of 1A

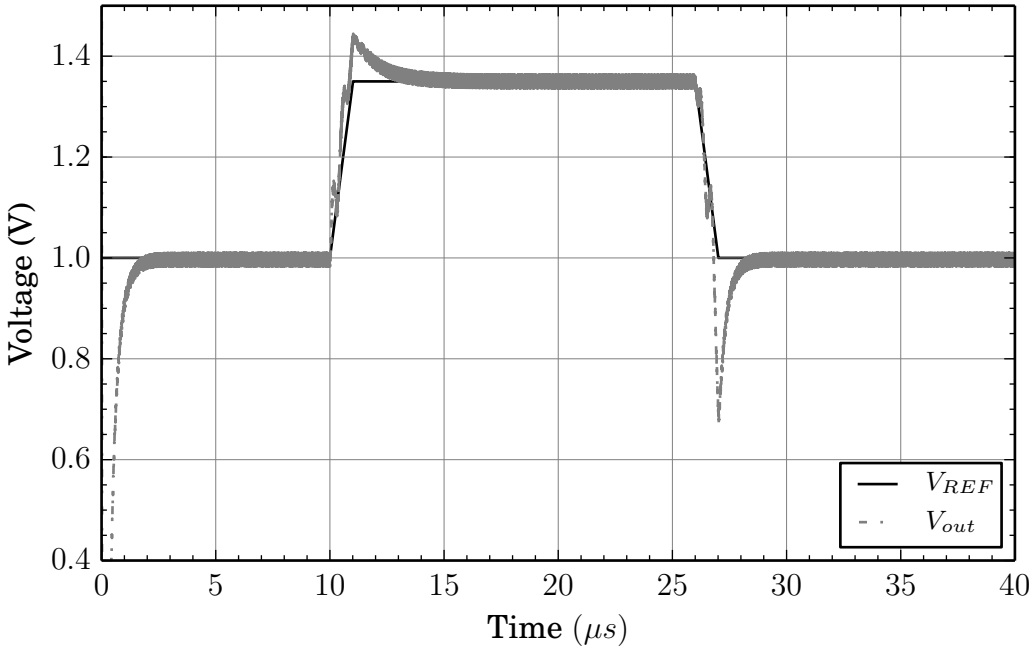


Figure 5.22: Rising pulse reference Transient. From 1.0V to 1.35V. Load of 1A

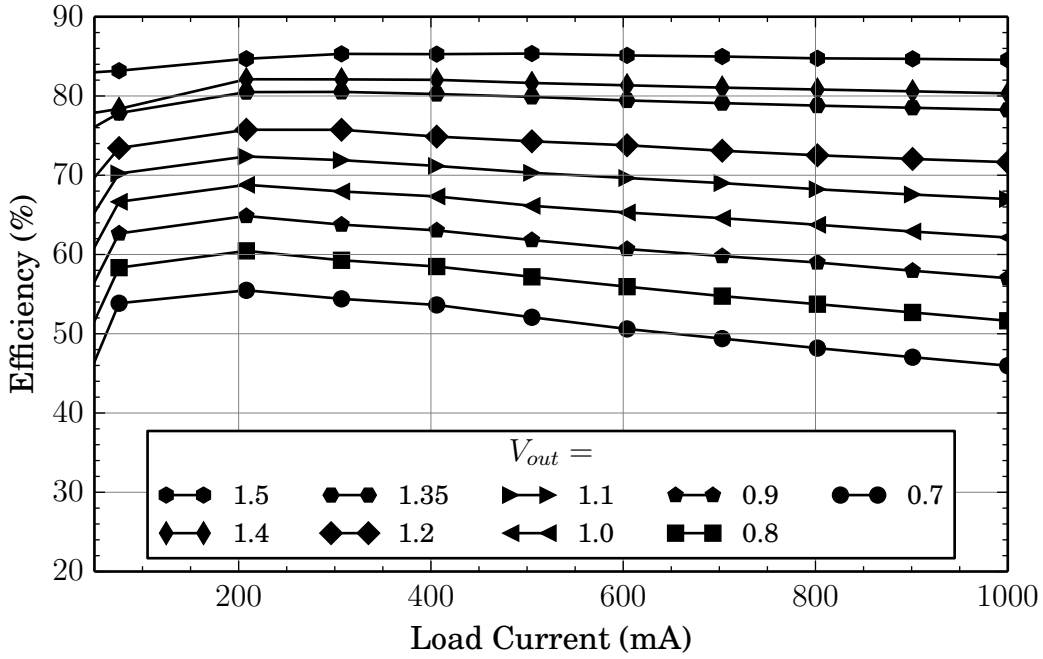


Figure 5.23: Efficiency as a function of load current or various output voltages

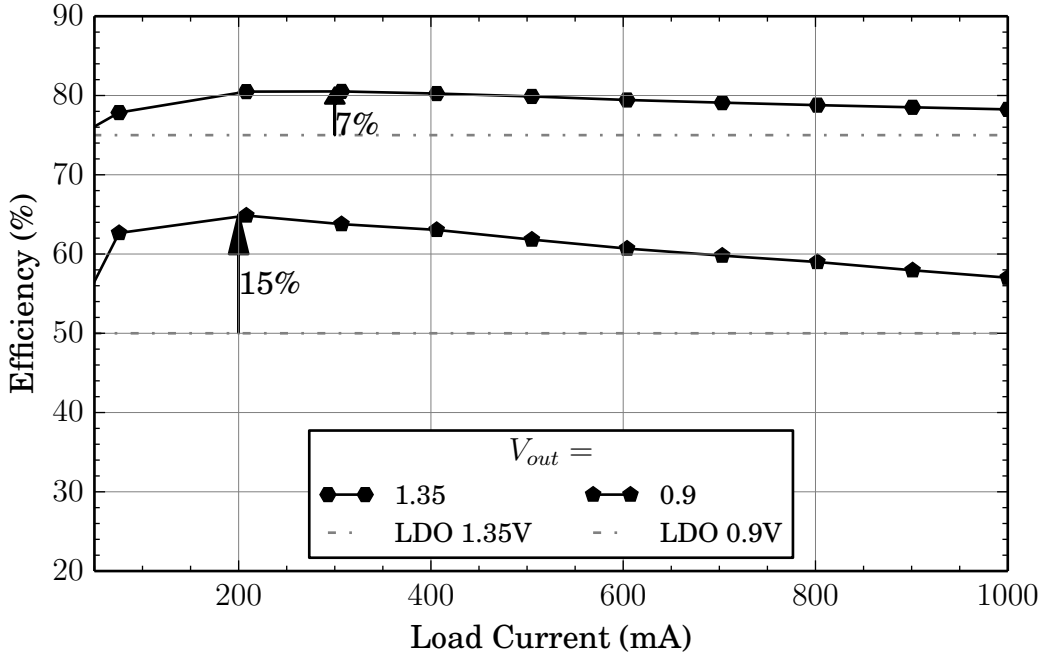


Figure 5.24: Inductive Converter Efficiency as compared to an ideal LDO

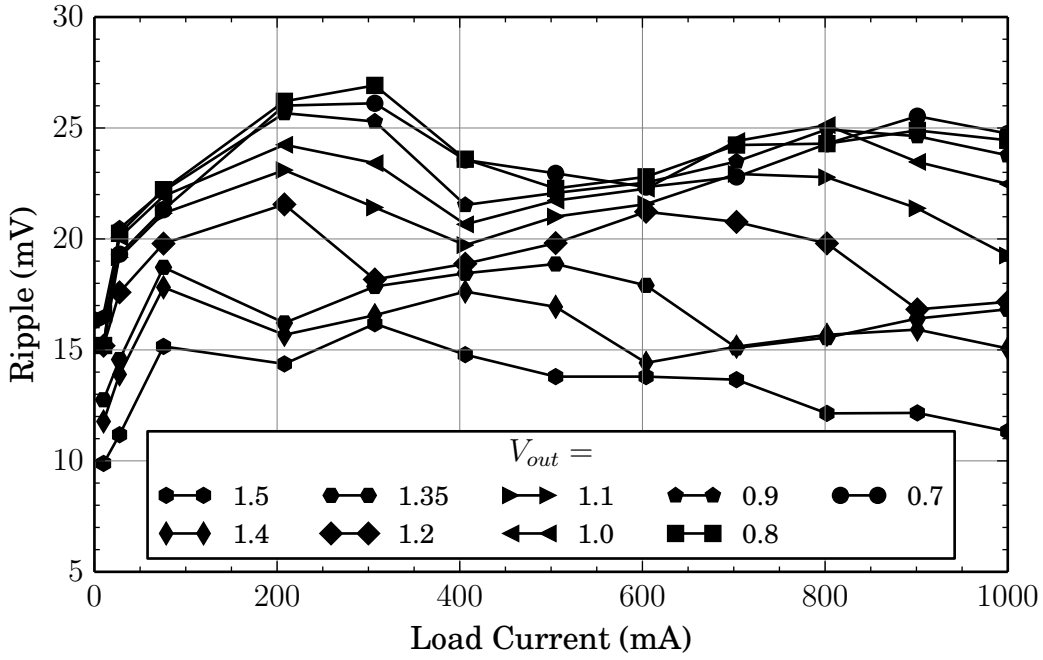


Figure 5.25: Ripple vs. Load Current for various output voltages

Table 5.2: Comparison of Inductive converter to works in the Literature

	[15]	[26]	[17]	[12]	[85]	This Work*
Year	2008	2011	2013	2013	2012	
Technology	0.13μm	0.13μm	0.13μm	0.13μm	0.13μm	0.15μm
Frequency	170MHz	200 - 300MHz	100MHz	100MHz	50 - 200	100MHz
Output Power	3 - 315	0.6 - 266	4 - 350	2.4 - 1260	12 - 1000	7 - 1400
Output Range	100X	450X	88X	525X	84X	200X
Input Voltage	1.2	1.2	1.2	1.2	2.4	1.8
Output Voltage	0.3-0.9	0.3 - 0.88	0.4 - 1.0	0.6 - 1.05	0.4 - 1.0	0.7 - 1.4
Efficiency	77.9	77	84.7	82.4	77	82
Inductor	On-Chip Spiral 2 x 2nH	Stacked Spiral 2nH	Bondwire >3nH	Bondwire 3 - 8nH	On-Chip Spiral 4 x 1nH	Bondwire 4 x 2nH
Capacitor	4.3 + 5.2nF	5nF	4.8 + 9.8nF	3.73nF	18 + 10nF	2 + 10nF
Area	1.5	1.59	2.25	1.25	5	3

* Simulated. Area is an estimate

5.6 Conclusion

In this chapter an inductive converter some of the results of the simulations were presented. In general the performance in terms of efficiency and ripple is comparable to other similar fully integrated converters. There transient startup and recovery times are mostly acceptable except for the voltage droops which need improvement.

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APPENDIX
EXAMPLE OF MNA-SS-REDOX STATE SPACE ANALYSIS OUTPUT

Input Netlist and Switching Sequence

$$\mathbf{N} = \begin{bmatrix} \text{xV} & 1 & 0 & V_{in} \\ \text{xS} & 1 & 2 & R_p \\ \text{xS} & 2 & 0 & R_n \\ \text{xL} & 2 & 3 & L \\ \text{xC} & 3 & 0 & C_L \\ \text{xS} & 1 & 4 & R_{S1} \\ \text{xS} & 4 & 3 & R_{S2} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 5 & 3 & R_{S4} \\ \text{xS} & 5 & 6 & R_{S5} \\ \text{xS} & 1 & 6 & R_{S6} \\ \text{xS} & 6 & 3 & R_{S7} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xS} & 7 & 3 & R_{S9} \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.1}$$

$$\mathbf{SSeq} = \begin{bmatrix} 0 & 0 & 1 & 0 & 1 & 0 & 0 & 1 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 0 \end{bmatrix} \tag{.2}$$

Phase Number 1

Preparaton Stage

OFF Switch Removal:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xV} & 1 & 0 & V_{in} \\ \text{xL} & 2 & 3 & L \\ \text{xC} & 3 & 0 & C_L \\ \text{xS} & 1 & 4 & R_{S1} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 1 & 6 & R_{S6} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.3}$$

Dead Branch Elimination: Dead Branches Found

$$\mathbf{Dead} = L \tag{.4}$$

Netlist After Dead Branch Removal:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xV} & 1 & 0 & V_{in} \\ \text{xC} & 3 & 0 & C_L \\ \text{xS} & 1 & 4 & R_{S1} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 1 & 6 & R_{S6} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.5}$$

Check Source Connections: Source Connected. OK
Netlist at Output of Preparation Stage:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xV} & 1 & 0 & V_{in} \\ \text{xC} & 3 & 0 & C_L \\ \text{xS} & 1 & 4 & R_{S1} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 1 & 6 & R_{S6} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.6}$$

MNA Stage

Sorted Netlist:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xC} & 3 & 0 & C_L \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xS} & 1 & 4 & R_{S1} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 1 & 6 & R_{S6} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xV} & 1 & 0 & V_{in} \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.7}$$

Incidence Matrix:

$$\mathbf{A} = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 1 & 0 & -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 & 0 \end{bmatrix} \tag{.8}$$

Sub matrices of Incidence Matrix:

$$\mathbf{A1} = \begin{bmatrix} 0 & 0 & 0 & 1 & 0 & 1 & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & -1 \end{bmatrix} \quad \mathbf{A2} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \quad \mathbf{A3} = \begin{bmatrix} 0 \\ 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{.9}$$

Group 1 Admittance Matrix Y1:

$$\mathbf{Y_1} = \begin{bmatrix} C_L\, D & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_1\, D & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_2\, D & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_{S1}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R_{S3}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{S6}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{S8}} \end{bmatrix} \tag{.10}$$

Group 2 Matrices $\mathbf{Y_2 V_2} + \mathbf{Z_2 I_2} = \mathbf{W_2}$:

$$\mathbf{Y_2} = 1 \quad \mathbf{Z_2} = 0 \quad \mathbf{W_2} = V_{in} \tag{.11}$$

Group 3 Current vector :

$$\mathbf{J_3} = I_{out} \tag{.12}$$

MNA Matrix System $\mathbf{TX} = \mathbf{U}$:

$$\begin{bmatrix} \frac{1}{R_{S1}} + \frac{1}{R_{S6}} & 0 & -\frac{1}{R_{S1}} & 0 & -\frac{1}{R_{S6}} & 0 & 1 \\ 0 & C_L\,D & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{R_{S1}} & 0 & \frac{1}{R_{S1}} + C_1\,D & -C_1\,D & 0 & 0 & 0 \\ 0 & 0 & -C_1\,D & \frac{1}{R_{S3}} + C_1\,D & 0 & 0 & 0 \\ -\frac{1}{R_{S6}} & 0 & 0 & 0 & \frac{1}{R_{S6}} + C_2\,D & -C_2\,D & 0 \\ 0 & 0 & 0 & 0 & -C_2\,D & \frac{1}{R_{S8}} + C_2\,D & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{n1} \\ V_{n3} \\ V_n4 \\ V_n5 \\ V_n6 \\ V_n7 \\ I_{Vin} \end{bmatrix} = \begin{bmatrix} 0 \\ -I_{out} \\ 0 \\ 0 \\ 0 \\ 0 \\ V_{in} \end{bmatrix} \tag{.13}$$

MNA to SS Stage

Seperate MNA System Matrix $\mathbf{T} = \mathbf{G} + \mathbf{CD}$:

$$\mathbf{G} = \begin{bmatrix} \frac{1}{R_{S1}} + \frac{1}{R_{S6}} & 0 & -\frac{1}{R_{S1}} & 0 & -\frac{1}{R_{S6}} & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ -\frac{1}{R_{S1}} & 0 & \frac{1}{R_{S1}} & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_{S3}} & 0 & 0 & 0 \\ -\frac{1}{R_{S6}} & 0 & 0 & 0 & \frac{1}{R_{S6}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{S8}} & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \mathbf{C} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_L & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_1 & -C_1 & 0 & 0 & 0 \\ 0 & 0 & -C_1 & C_1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & C_2 & -C_2 & 0 \\ 0 & 0 & 0 & 0 & -C_2 & C_2 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \tag{.14}$$

Seperate MNA Excitation vector $\mathbf{U} = \mathbf{KS}$:

$$\mathbf{K} = \begin{bmatrix} 0 & 0 \\ 0 & -1 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 1 & 0 \end{bmatrix} \mathbf{S} = \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix} \tag{.15}$$

Row Echelon Form Operations Matrix:

$$\mathbf{Ops} = \begin{bmatrix} 0 & \frac{1}{C_L} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_2} & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{.16}$$

G C and K after Row Operations:

$$\mathbf{G} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1 R_{S3}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_2 R_{S8}} & 0 \\ \frac{1}{R_{S1}} + \frac{1}{R_{S6}} & 0 & -\frac{1}{R_{S1}} & 0 & -\frac{1}{R_{S6}} & 0 & 1 \\ -\frac{1}{R_{S1}} & 0 & \frac{1}{R_{S1}} & \frac{1}{R_{S3}} & 0 & 0 & 0 \\ -\frac{1}{R_{S6}} & 0 & 0 & 0 & \frac{1}{R_{S6}} & \frac{1}{R_{S8}} & 0 \\ 1 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \mathbf{C} = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & -1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad \mathbf{K} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 1 & 0 \end{bmatrix} \tag{.17}$$

Pivoting Vector:

$$\mathbf{Piv} = \begin{bmatrix} 2 & 3 & 5 & 1 & 4 & 6 & 7 \end{bmatrix} \tag{.18}$$

G C and X after Pivoting:

$$\mathbf{G} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_1 R_{S3}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & -\frac{1}{C_2 R_{S8}} & 0 \\ 0 & -\frac{1}{R_{S1}} & -\frac{1}{R_{S6}} & \frac{1}{R_{S1}} + \frac{1}{R_{S6}} & 0 & 0 & 1 \\ 0 & \frac{1}{R_{S1}} & 0 & -\frac{1}{R_{S1}} & \frac{1}{R_{S3}} & 0 & 0 \\ 0 & 0 & \frac{1}{R_{S6}} & -\frac{1}{R_{S6}} & 0 & \frac{1}{R_{S8}} & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 \end{bmatrix} \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & -1 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad \mathbf{X} = \begin{bmatrix} V_{n3} \\ V_n 4 \\ V_n 6 \\ V_{n1} \\ V_n 5 \\ V_n 7 \\ I_{Vin} \end{bmatrix} \tag{.19}$$

Partitioning of Matrices G, C, K, X :

$$\mathbf{G_{11}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad \mathbf{G_{12}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{C_1 R_{S3}} & 0 & 0 \\ 0 & 0 & -\frac{1}{C_2 R_{S8}} & 0 \end{bmatrix} \quad \mathbf{G_{21}} = \begin{bmatrix} 0 & -\frac{1}{R_{S1}} & -\frac{1}{R_{S6}} \\ 0 & \frac{1}{R_{S1}} & 0 \\ 0 & 0 & \frac{1}{R_{S6}} \\ 0 & 0 & 0 \end{bmatrix} \quad \mathbf{G_{22}} = \begin{bmatrix} \frac{1}{R_{S1}} + \frac{1}{R_{S6}} & 0 & 0 & 1 \\ -\frac{1}{R_{S1}} & \frac{1}{R_{S3}} & 0 & 0 \\ -\frac{1}{R_{S6}} & 0 & \frac{1}{R_{S8}} & 0 \\ 1 & 0 & 0 & 0 \end{bmatrix} \tag{.20}$$

$$\mathbf{C_{11}} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad \mathbf{C_{12}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 \\ 0 & 0 & -1 & 0 \end{bmatrix} \quad \mathbf{C_{21}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad \mathbf{C_{22}} = \begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \tag{.21}$$

$$\mathbf{K_{11}} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \qquad \mathbf{K_{12}} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 1 & 0 \end{bmatrix} \tag{.22}$$

$$\mathbf{X_1} = \begin{bmatrix} V_{n3} \\ V_n4 \\ V_n6 \end{bmatrix} \qquad \mathbf{X_2} = \begin{bmatrix} V_{n1} \\ V_n5 \\ V_n7 \\ I_{Vin} \end{bmatrix} \tag{.23}$$

Reduced System Coefficients G1, C1, K1

$$\mathbf{C1} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & \frac{R_{S3}}{R_{S1}} + 1 & 0 \\ 0 & 0 & \frac{R_{S8}}{R_{S6}} + 1 \end{bmatrix} \quad \mathbf{G1} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & \frac{1}{C_1 R_{S1}} & 0 \\ 0 & 0 & \frac{1}{C_2 R_{S6}} \end{bmatrix} \quad \mathbf{K1} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ \frac{1}{C_1 R_{S1}} & 0 \\ \frac{1}{C_2 R_{S6}} & 0 \end{bmatrix} \quad \mathbf{K2} = \begin{bmatrix} 0 & 0 \\ \frac{R_{S3}}{R_{S1}} & 0 \\ \frac{R_{S8}}{R_{S6}} & 0 \end{bmatrix} \tag{.24}$$

State Space Equations $\mathbf{dX/dt} = \mathbf{A_S X} + \mathbf{B_S S}$:

$$\mathbf{X} = \begin{bmatrix} V_{n3} \\ V_n4 \\ V_n6 \end{bmatrix} \mathbf{A_S} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{C_1 [R_{S1}+R_{S3}]} & 0 \\ 0 & 0 & -\frac{1}{C_2 [R_{S6}+R_{S8}]} \end{bmatrix} \quad \mathbf{B_S} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ \frac{1}{C_1 [R_{S1}+R_{S3}]} & 0 \\ \frac{1}{C_2 [R_{S6}+R_{S8}]} & 0 \end{bmatrix} \tag{.25}$$

Phase Number 2

Preparaton Stage

OFF Switch Removal:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xV} & 1 & 0 & V_{in} \\ \text{xL} & 2 & 3 & L \\ \text{xC} & 3 & 0 & C_L \\ \text{xS} & 4 & 3 & R_{S2} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 6 & 3 & R_{S7} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.26}$$

Dead Branch Elimination: Dead Branches Found

$$\mathbf{Dead} = L \tag{.27}$$

Netlist After Dead Branch Removal:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xV} & 1 & 0 & V_{in} \\ \text{xC} & 3 & 0 & C_L \\ \text{xS} & 4 & 3 & R_{S2} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 6 & 3 & R_{S7} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.28}$$

Check Source Connections: Source Disconnected. Remove Source

Netlist at Output of Preparation Stage:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xC} & 3 & 0 & C_L \\ \text{xS} & 4 & 3 & R_{S2} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 6 & 3 & R_{S7} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.29}$$

MNA Stage

Sorted Netlist:

$$\mathbf{N_{tmp}} = \begin{bmatrix} \text{xC} & 3 & 0 & C_L \\ \text{xC} & 4 & 5 & C_1 \\ \text{xC} & 6 & 7 & C_2 \\ \text{xS} & 4 & 3 & R_{S2} \\ \text{xS} & 0 & 5 & R_{S3} \\ \text{xS} & 6 & 3 & R_{S7} \\ \text{xS} & 0 & 7 & R_{S8} \\ \text{xJ} & 3 & 0 & I_{out} \end{bmatrix} \tag{.30}$$

Incidence Matrix:

$$\mathbf{A} = \begin{bmatrix} 1 & 0 & 0 & -1 & 0 & -1 & 0 & 1 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & -1 & 0 \end{bmatrix} \tag{.31}$$

Sub matrices of Incidence Matrix:

$$\mathbf{A1} = \begin{bmatrix} 1 & 0 & 0 & -1 & 0 & -1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 & 0 \\ 0 & -1 & 0 & 0 & -1 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 & 0 \\ 0 & 0 & -1 & 0 & 0 & 0 & -1 \end{bmatrix} \quad \mathbf{A2} = [] \quad \mathbf{A3} = \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{.32}$$

Group 1 Admittance Matrix Y1:

$$\mathbf{Y_1} = \begin{bmatrix} C_L\, D & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & C_1\, D & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & C_2\, D & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{R_{S2}} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R_{S3}} & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{S7}} & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & \frac{1}{R_{S8}} \end{bmatrix} \tag{.33}$$

Group 2 Matrices $\mathbf{Y_2V_2} + \mathbf{Z_2I_2} = \mathbf{W_2}$:

$$\mathbf{Y_2} = [] \quad \mathbf{Z_2} = [] \quad \mathbf{W_2} = [] \tag{.34}$$

Group 3 Current vector :

$$\mathbf{J_3} = I_{out} \tag{.35}$$

MNA Matrix System $\mathbf{TX} = \mathbf{U}$:

$$\begin{bmatrix} \frac{1}{R_{S2}} + \frac{1}{R_{S7}} + C_L\,D & -\frac{1}{R_{S2}} & 0 & -\frac{1}{R_{S7}} & 0 \\ -\frac{1}{R_{S2}} & \frac{1}{R_{S2}} + C_1\,D & -C_1\,D & 0 & 0 \\ 0 & -C_1\,D & \frac{1}{R_{S3}} + C_1\,D & 0 & 0 \\ -\frac{1}{R_{S7}} & 0 & 0 & \frac{1}{R_{S7}} + C_2\,D & -C_2\,D \\ 0 & 0 & 0 & -C_2\,D & \frac{1}{R_{S8}} + C_2\,D \end{bmatrix} \begin{bmatrix} V_{n3} \\ V_n4 \\ V_n5 \\ V_n6 \\ V_n7 \end{bmatrix} = \begin{bmatrix} -I_{out} \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix} \tag{.36}$$

MNA to SS Stage

Seperate MNA System Matrix $\mathbf{T} = \mathbf{G} + \mathbf{CD}$:

$$\mathbf{G} = \begin{bmatrix} \frac{1}{R_{S2}} + \frac{1}{R_{S7}} & -\frac{1}{R_{S2}} & 0 & -\frac{1}{R_{S7}} & 0 \\ -\frac{1}{R_{S2}} & \frac{1}{R_{S2}} & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{R_{S3}} & 0 & 0 \\ -\frac{1}{R_{S7}} & 0 & 0 & \frac{1}{R_{S7}} & 0 \\ 0 & 0 & 0 & 0 & \frac{1}{R_{S8}} \end{bmatrix} \mathbf{C} = \begin{bmatrix} C_L & 0 & 0 & 0 & 0 \\ 0 & C_1 & -C_1 & 0 & 0 \\ 0 & -C_1 & C_1 & 0 & 0 \\ 0 & 0 & 0 & C_2 & -C_2 \\ 0 & 0 & 0 & -C_2 & C_2 \end{bmatrix} \tag{.37}$$

Seperate MNA Excitation vector $\mathbf{U} = \mathbf{KS}$:

$$\mathbf{K} = \begin{bmatrix} 0 & -1 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \mathbf{S} = \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix} \tag{.38}$$

Row Echelon Form Operations Matrix:

$$\mathbf{Ops} = \begin{bmatrix} \frac{1}{C_L} & 0 & 0 & 0 & 0 \\ 0 & 0 & -\frac{1}{C_1} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_2} \\ 0 & 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 1 \end{bmatrix} \tag{.39}$$

G C and K after Row Operations:

$$\mathbf{G} = \begin{bmatrix} \frac{\frac{1}{R_{S2}}+\frac{1}{R_{S7}}}{C_L} & -\frac{1}{C_L R_{S2}} & 0 & -\frac{1}{C_L R_{S7}} & 0 \\ 0 & 0 & -\frac{1}{C_1 R_{S3}} & 0 & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_2 R_{S8}} \\ -\frac{1}{R_{S2}} & \frac{1}{R_{S2}} & \frac{1}{R_{S3}} & 0 & 0 \\ -\frac{1}{R_{S7}} & 0 & 0 & \frac{1}{R_{S7}} & \frac{1}{R_{S8}} \end{bmatrix} \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \\ 0 & 0 & 0 & 1 & -1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad \mathbf{K} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{.40}$$

Pivoting Vector:

$$\mathbf{Piv} = \begin{bmatrix} 1 & 2 & 4 & 3 & 5 \end{bmatrix} \tag{.41}$$

G C and X after Pivoting:

$$\mathbf{G} = \begin{bmatrix} \frac{\frac{1}{R_{S2}}+\frac{1}{R_{S7}}}{C_L} & -\frac{1}{C_L R_{S2}} & -\frac{1}{C_L R_{S7}} & 0 & 0 \\ 0 & 0 & 0 & -\frac{1}{C_1 R_{S3}} & 0 \\ 0 & 0 & 0 & 0 & -\frac{1}{C_2 R_{S8}} \\ -\frac{1}{R_{S2}} & \frac{1}{R_{S2}} & 0 & \frac{1}{R_{S3}} & 0 \\ -\frac{1}{R_{S7}} & 0 & \frac{1}{R_{S7}} & 0 & \frac{1}{R_{S8}} \end{bmatrix} \mathbf{C} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & -1 & 0 \\ 0 & 0 & 1 & 0 & -1 \\ 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \quad \mathbf{X} = \begin{bmatrix} V_n 3 \\ V_n 4 \\ V_n 6 \\ V_n 5 \\ V_n 7 \end{bmatrix} \tag{.42}$$

Partitioning of Matrices G, C, K, X :

$$\mathbf{G_{11}} = \begin{bmatrix} \frac{\frac{1}{R_{S2}}+\frac{1}{R_{S7}}}{C_L} & -\frac{1}{C_L R_{S2}} & -\frac{1}{C_L R_{S7}} \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad \mathbf{G_{12}} = \begin{bmatrix} 0 & 0 \\ -\frac{1}{C_1 R_{S3}} & 0 \\ 0 & -\frac{1}{C_2 R_{S8}} \end{bmatrix} \quad \mathbf{G_{21}} = \begin{bmatrix} -\frac{1}{R_{S2}} & \frac{1}{R_{S2}} & 0 \\ -\frac{1}{R_{S7}} & 0 & \frac{1}{R_{S7}} \end{bmatrix} \quad \mathbf{G_{22}} = \begin{bmatrix} \frac{1}{R_{S3}} & 0 \\ 0 & \frac{1}{R_{S8}} \end{bmatrix} \tag{.43}$$

$$\mathbf{C_{11}} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad \mathbf{C_{12}} = \begin{bmatrix} 0 & 0 \\ -1 & 0 \\ 0 & -1 \end{bmatrix} \quad \mathbf{C_{21}} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix} \quad \mathbf{C_{22}} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{.44}$$

$$\mathbf{K_{11}} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad \mathbf{K_{12}} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{.45}$$

$$\mathbf{X_1} = \begin{bmatrix} V_n3 \\ V_n4 \\ V_n6 \end{bmatrix} \quad \mathbf{X_2} = \begin{bmatrix} V_n5 \\ V_n7 \end{bmatrix} \tag{.46}$$

Reduced System Coefficients G1, C1, K1

$$\mathbf{C1} = \begin{bmatrix} 1 & 0 & 0 \\ -\frac{R_{S3}}{R_{S2}} & \frac{R_{S3}}{R_{S2}}+1 & 0 \\ -\frac{R_{S8}}{R_{S7}} & 0 & \frac{R_{S8}}{R_{S7}}+1 \end{bmatrix} \quad \mathbf{G1} = \begin{bmatrix} \frac{\frac{1}{R_{S2}}+\frac{1}{R_{S7}}}{C_L} & -\frac{1}{C_L R_{S2}} & -\frac{1}{C_L R_{S7}} \\ -\frac{1}{C_1 R_{S2}} & \frac{1}{C_1 R_{S2}} & 0 \\ -\frac{1}{C_2 R_{S7}} & 0 & \frac{1}{C_2 R_{S7}} \end{bmatrix} \quad \mathbf{K1} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \quad \mathbf{K2} = \begin{bmatrix} 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{bmatrix} \tag{.47}$$

State Space Equations $\mathbf{dX/dt} = \mathbf{A_S X} + \mathbf{B_S S}$:

$$\mathbf{X} = \begin{bmatrix} V_{n3} \\ V_n4 \\ V_n6 \end{bmatrix} \mathbf{A_S} = \begin{bmatrix} -\frac{R_{S2}+R_{S7}}{C_L\,R_{S2}\,R_{S7}} & \frac{1}{C_L\,R_{S2}} & \frac{1}{C_L\,R_{S7}} \\ -\frac{C_1\,R_{S2}\,R_{S3}+C_1\,R_{S3}\,R_{S7}-C_L\,R_{S2}\,R_{S7}}{C_1\,C_L\,R_{S2}\,R_{S7}\,[R_{S2}+R_{S3}]} & \frac{C_1\,R_{S3}-C_L\,R_{S2}}{C_1\,C_L\,R_{S2}\,[R_{S2}+R_{S3}]} & \frac{R_{S3}}{C_L\,R_{S7}\,[R_{S2}+R_{S3}]} \\ -\frac{C_2\,R_{S2}\,R_{S8}+C_2\,R_{S7}\,R_{S8}-C_L\,R_{S2}\,R_{S7}}{C_2\,C_L\,R_{S2}\,R_{S7}\,[R_{S7}+R_{S8}]} & \frac{R_{S8}}{C_L\,R_{S2}\,[R_{S7}+R_{S8}]} & \frac{C_2\,R_{S8}-C_L\,R_{S7}}{C_2\,C_L\,R_{S7}\,[R_{S7}+R_{S8}]} \end{bmatrix} \quad \mathbf{B_S} = \begin{bmatrix} 0 & -\frac{1}{C_L} \\ 0 & -\frac{R_{S3}}{C_L\,[R_{S2}+R_{S3}]} \\ 0 & -\frac{R_{S8}}{C_L\,[R_{S7}+R_{S8}]} \end{bmatrix} \tag{.48}$$

Phase 1

$$\frac{d}{dt}\begin{bmatrix} V_{n3} \\ V_n4 \\ V_n6 \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & -\frac{1}{C_1\,[R_{S1}+R_{S3}]} & 0 \\ 0 & 0 & -\frac{1}{C_2\,[R_{S6}+R_{S8}]} \end{bmatrix} \begin{bmatrix} V_{n3} \\ V_n4 \\ V_n6 \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{C_L} \\ \frac{1}{C_1\,[R_{S1}+R_{S3}]} & 0 \\ \frac{1}{C_2\,[R_{S6}+R_{S8}]} & 0 \end{bmatrix} \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix} \tag{.49}$$

Phase 2

$$\frac{d}{dt}\begin{bmatrix} V_{n3} \\ V_n4 \\ V_n6 \end{bmatrix} = \begin{bmatrix} -\frac{R_{S2}+R_{S7}}{C_L\,R_{S2}\,R_{S7}} & \frac{1}{C_L\,R_{S2}} & \frac{1}{C_L\,R_{S7}} \\ -\frac{C_1\,R_{S2}\,R_{S3}+C_1\,R_{S3}\,R_{S7}-C_L\,R_{S2}\,R_{S7}}{C_1\,C_L\,R_{S2}\,R_{S7}\,[R_{S2}+R_{S3}]} & \frac{C_1\,R_{S3}-C_L\,R_{S2}}{C_1\,C_L\,R_{S2}\,[R_{S2}+R_{S3}]} & \frac{R_{S3}}{C_L\,R_{S7}\,[R_{S2}+R_{S3}]} \\ -\frac{C_2\,R_{S2}\,R_{S8}+C_2\,R_{S7}\,R_{S8}-C_L\,R_{S2}\,R_{S7}}{C_2\,C_L\,R_{S2}\,R_{S7}\,[R_{S7}+R_{S8}]} & \frac{R_{S8}}{C_L\,R_{S2}\,[R_{S7}+R_{S8}]} & \frac{C_2\,R_{S8}-C_L\,R_{S7}}{C_2\,C_L\,R_{S7}\,[R_{S7}+R_{S8}]} \end{bmatrix} \begin{bmatrix} V_{n3} \\ V_n4 \\ V_n6 \end{bmatrix} + \begin{bmatrix} 0 & -\frac{1}{C_L} \\ 0 & -\frac{R_{S3}}{C_L\,[R_{S2}+R_{S3}]} \\ 0 & -\frac{R_{S8}}{C_L\,[R_{S7}+R_{S8}]} \end{bmatrix} \begin{bmatrix} V_{in} \\ I_{out} \end{bmatrix} \tag{.50}$$

VITAE

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  - Mohanad Ahmed, Mohammad AlGhamdi "A Modified Rail to Rail Input Goll-Zimmerman Comparator for Low Voltage Applications" *to be Submitted*